Latest Advances and Future Prospects of STT-RAM

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Grandis, Inc.

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• Grandis Corporation Overview

• Introduction to STT-RAM*

• Latest STT-RAM Device & Chip Results

• STT-RAM Market & Applications

• Conclusions

*STT-RAM: Spin Transfer Torque Random Access Memory
Grandis Corporation Overview

• **Grandis develops & licenses STT-RAM proprietary NVM solutions**
  – Grandis’ non-volatile STT-RAM enables a wide variety of low-cost and high-performance memory products at the 45 nm technology node and beyond

• **Incorporated in Delaware in 2002**

• **Top-tier VC Funded**
  – Sevin Rosen, Applied Ventures, Matrix Partners, Incubic, Concept Ventures

• **Headquarters: Silicon Valley, CA**
  – R & D Offices: California, Japan, S. Korea

• **Strong & broad STT-RAM patent portfolio and know-how**
  – 52 patents granted to date in U.S.
  – Total 193 patents filed and 63 granted worldwide

• **Our mission is to establish Grandis STT-RAM as the #1 choice for memory solutions beyond 45 nm**

STT-RAM: Spin Transfer Torque Random Access Memory
Grandis Milestones in STT-RAM

2002: Grandis files first key patents in STT-RAM

2004: Grandis reports world’s first STT switching in MTJs

2005: Renesas Technology of Japan licenses Grandis IP and begins developing STT-RAM for embedded applications

2007: Grandis receives Technology Innovation Award from Frost & Sullivan
      Grandis wins NIST ATP award ($2M / 3 yrs) to develop STT-RAM

2008: Hynix Semiconductor of Korea licenses Grandis IP and begins developing STT-RAM for standalone applications
      Grandis wins DARPA contract ($15M / 4 yrs) to develop STT-RAM

2009: Grandis upgrades MTJ Fab to handle 300 mm customer wafers
      Grandis wins two additional NSF Grants worth $1M
      Grandis awarded its 50th patent in the U.S.

2010: Grandis achieves DARPA Phase I development milestones 6 months early
The Need for a New Memory Technology

- All existing memory technology is greatly challenged beyond 45 nm
  - SRAM: high power consumption, leakage increasing 10X with each technology node
  - DRAM: refresh current increasing, incompatible process for embedded applications
  - Flash: limited endurance, high write power, very slow write speed, MLC & aggressive scaling leading to reduced performance and complicated controller

- Power consumption in both mobile and data center applications is now a real issue
  - Incorporating STT-RAM in mobile applications can dramatically reduce standby power
  - Replacing DRAM with STT-RAM in data centers can reduce power by up to 75%

- Memory performance is fast becoming the key bottleneck that limits system performance
  - Critical applications are becoming more data-centric, less compute-centric
  - Instant-on is becoming a requirement for many applications

- These problems create an opening for an alternative, high-density, high-speed, non-volatile random access memory
The Solution: STT-RAM Universal Memory

• **STT-RAM** is an evolution in magnetic storage from hard disk drives to solid-state semiconductor memory
  – Uses spin-polarized current ("spintronics") to write magnetic bits
  – Non-volatile, random-access memory with no moving parts
  – Key building block is the magnetic tunnel junction (MTJ)

• **STT-RAM** has all the characteristics of a universal memory
  – Non-volatile
  – Highly scalable
  – Low power consumption
  – SRAM read/write speed
  – Unlimited endurance
  – DRAM & Flash density (6 F²)
  – Multi-level cell capability

• **STT-RAM** uses existing CMOS technology with 2 additional masks and less than 3% cost adder
Key Advantages over conventional MRAM:

- **Excellent write selectivity**  
  - Localized spin-injection within cell
- **High scalability**  
  - Write current scales down with cell size
- **Low power consumption**  
  - Low write current (<100 μA)
- **Simpler architecture**  
  - No write line, no by-pass line and no cladding
- **Faster operation**  
  - Multibit (parallel) writing compatible
STT Write Mechanism

- **Spin-transfer torque writing**
  - Uses spin-polarized current instead of magnetic field to switch magnetization of storage layer
  - Has low power consumption and excellent scalability
STT-RAM Key Parameters

- **Jc0** (write current density) => cell size, write speed
- **TMR** (read signal) => sense margin, read speed
- **Δ** (thermal stability) => data retention, read disturb, memory size, temperature range
- **Vbd** (MTJ breakdown voltage) => lifetime, endurance

- Key challenge is achieving low STT write current density and high thermal stability at the same time

- **Write current:**
  \[ I_{c0} = \frac{2\alpha AM^*_S t_F e}{\eta \hbar} \left[ H_K + \frac{H_d}{2} \right], \quad H_K = H_{Intrinsic} + H_{shape} + \ldots \]

- **Thermal stability:**
  \[ \Delta = \frac{M^*_S H_K t_F A}{2k_B T} \propto \frac{M^*_S t_F^2 A}{k_B T} \]

  Assuming intrinsic anisotropy is much smaller than shape anisotropy
Latest MTJ Device Results

- New class of in-plane MTJ structures with high partial perpendicular are excellent for maintaining thermal stability as device sizes shrink

- **Average write current density** $J_{c0}$ **for advanced MTJs is in range 1–2 MA/cm$^2$**
  - Dual barrier MTJ (DMTJ) devices provide the lowest average write current density of $\sim 1$ MA/cm$^2$

Each $J_{c0}$ data point is obtained statistically by fitting write current vs device area data from thousands of MTJs over a wide range of device sizes.
STT-RAM Scalability

- **New micromagnetic simulations show in-plane STT-RAM scalable beyond 20 nm**
  - Key issue is maintaining thermal stability as device area shrinks (e.g. by increasing free layer thickness or aspect ratio)

**Simple Scaling**

$$\text{Write current } I_c \approx w^2$$

**Thermal stability } \Delta \approx w$$

**Scaling at Fixed } \Delta = 60**

<table>
<thead>
<tr>
<th>Simple Scaling</th>
<th>In-plane STT-RAM</th>
<th>Perpendicular STT-RAM</th>
</tr>
</thead>
<tbody>
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<td>Write current $I_c$</td>
<td>$\approx w^2$</td>
<td>$\approx w^2$</td>
</tr>
<tr>
<td>Thermal stability $\Delta$</td>
<td>$\approx w$</td>
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<tr>
<td>Write current $I_c$</td>
<td>$\approx w^{3/2}$</td>
<td>Constant</td>
</tr>
<tr>
<td>Thermal stability $\Delta$</td>
<td>Constant</td>
<td>Constant</td>
</tr>
</tbody>
</table>
STT-RAM Minimum Cell Size

- **6 F^2 minimum cell size with shared source line architecture**
  - Minimum 1 F gate width transistor can drive 6 F^2 cell beyond 45 nm

- **Future multi-level cell and cross-point architectures will enable further scaling beyond 6 F^2**
Grandis STT-RAM Chip

- The most advanced STT-RAM prototype chip in the industry
  - Fully-functional
  - 256 kbit capacity
  - 90 nm CMOS
  - 4 Cu metal process
  - LP high reliability CMOS
  - Write current <200 µA
  - Write/read speed 20 ns
  - Endurance >$10^{13}$

Higher density chips at 54 nm & beyond are in development
STT-RAM Resistance Distribution

- Large separation between resistance states and small process distribution provide excellent read characteristics
  - TMR (Tunneling Magnetoresistive) signal ~100%
  - R_{low} distribution sigma 4% (1\sigma), R_{high} distribution sigma 3% (1\sigma)
  - R_{high} – R_{low} separation = 20\sigma
STT-RAM Write Voltage Distribution

• Mean write voltage $\sim 1.15$ V
  – Includes voltage across both transistor and MTJ

• Write voltage distribution
  $\sim 3\% \ (1\sigma)$ or $\sim 9\% \ (3\sigma)$

• Grandis target write voltage distribution $< 15\% \ (3\sigma)$
• Unlimited write endurance (>10^{16} cycles) projected from TDDB tests with stressed voltage and temperature
  – 10^{13} endurance demonstrated to date under real operating conditions
Grandis STT-RAM will be in production in <2 years
- Initially, as an embedded SRAM & low power mobile RAM replacement
- In medium term, as a DRAM & NOR flash replacement
- Ultimately, as a storage class memory that can replace NAND Flash

STT-RAM total addressable market will be >$80B by 2015
STT-RAM can replace MCPs in mobile applications with a single chip
- Non-volatile, higher-speed, lower power consumption, and lower cost

Handset Solution
Sharp 922SH

Multi-Chip Package (MCP) (ST M39PNRA2A)
NOR: STMicro 512Mb 2pcs
NAND: Hynix 2Gb
    SLC(single-level-cell) 1Pcs
DRAM: Elpida 512Mb DDR2
    SDRAM 2Pcs
Smart Phone with Conventional Memory

Store & run radio protocol stack

on-chip level 1(2) cache sizes are a function of ext. memory access latency and required bandwidth

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Smart Phone with STT-RAM Memory

- Baseband/Modem
  - Memory Ctrl
  - x16 (mux) STT-RAM

- Application Processor
  - Memory Ctrl
  - x16 (mux) x16/x32 x8/x16

- Media Processor
  - ARM9

- Image sensor

- LCD Display

- RF

- On-chip STT-RAM Frame Buffer (e.g., 64Mb)

- On-chip level 1(2) cache sizes are a function of ext. memory access latency and required bandwidth

- Store & run radio protocol stack

- Serial i/f

- Audio/Video/TVout

- MMC/SD

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## Memory Technology Comparison

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>Flash (NOR)</th>
<th>Flash (NAND)</th>
<th>FeRAM</th>
<th>MRAM</th>
<th>PRAM</th>
<th>RRAM</th>
<th>STT-RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Non-volatile</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Cell size (F²)</strong></td>
<td>50–120</td>
<td>6–10</td>
<td>10</td>
<td>5</td>
<td>15–34</td>
<td>16–40</td>
<td>6–12</td>
<td>6–10</td>
<td>6–20</td>
</tr>
<tr>
<td><strong>Read time (ns)</strong></td>
<td>1–100</td>
<td>30</td>
<td>10</td>
<td>50</td>
<td>20–80</td>
<td>3–20</td>
<td>20–50</td>
<td>10–50</td>
<td>2–20</td>
</tr>
<tr>
<td><strong>Write / Erase time (ns)</strong></td>
<td>1–100</td>
<td>15</td>
<td>1 μs / 10 ms</td>
<td>1 ms / 0.1 ms</td>
<td>50 / 50</td>
<td>3–20</td>
<td>50 / 120</td>
<td>10–50</td>
<td>2–20</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>10¹⁶</td>
<td>10¹⁶</td>
<td>10⁵</td>
<td>10⁵</td>
<td>10¹²</td>
<td>&gt;10¹⁵</td>
<td>10⁸</td>
<td>10⁸</td>
<td>&gt;10¹⁵</td>
</tr>
<tr>
<td><strong>Write power</strong></td>
<td>Low</td>
<td>Low</td>
<td>Very high</td>
<td>Very high</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Other power consumption</strong></td>
<td>Current</td>
<td>Refresh</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td><strong>High voltage required</strong></td>
<td>No</td>
<td>3 V</td>
<td>6–8 V</td>
<td>16–20 V</td>
<td>2–3 V</td>
<td>3 V</td>
<td>1.5–3 V</td>
<td>1.5–3 V</td>
<td>&lt;1.5 V</td>
</tr>
</tbody>
</table>

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Intensified Worldwide Interest in STT-RAM

Jun. 2009: NEC tips new MRAM technology using STT at VLSI conference, expects it to be scalable beyond 55 nm process

Oct. 2009: Crocus Technology announces it will transition to STT-RAM from its existing heat-assisted TAS-MRAM in 2010

Nov. 2009: Korean Government updates on progress of $50M STT-RAM program with Samsung and Hynix, installs 300 mm STT-RAM facility at Hanyang University

Dec. 2009: TSMC and Qualcomm describe 45 nm low power embedded STT-RAM process and design at IEDM

Dec. 2009: Also at IEDM, Hitachi & Tohoku University present MTJ SPICE model, and Intel presents design space study and requirements for STT-RAM in embedded applications

Dec. 2009: France launches €4.2M SPIN project with 11 partners including LETI, Spintec & Crocus, one of project goals is to develop magnetic FPGAs

Jan. 2010: Everspin introduces 1 Mb MRAM for RAID storage applications

Jan. 2010: Toshiba achieves 9 µA switching current in perpendicular STT-RAM

Feb. 2010: Toshiba describes a 64 Mb STT-RAM using perpendicular MTJs and 65 nm CMOS at ISSCC conference, Fujitsu also presents a paper
**Conclusions**

- **Spintronics (spin electronics) is a rapidly emerging field**
  - STT-RAM and spin logic will have a significant impact on technology in the 21st century, enabling a new era of instant-on, high-speed portable devices with extended battery life

- **STT-RAM has a huge potential market as a universal, scalable memory**
  - It can replace eSRAM & eFlash at 45 nm, DRAM at 32 nm, and ultimately replace NAND Flash as a storage class memory at 22 nm and beyond

- **Worldwide STT-RAM development has increased significantly**
  - Government programs in the United States (DARPA), Korea, Japan & France
  - IBM, Qualcomm, Intel, Everspin, TSMC, Hynix, Samsung, Renesas, NEC, Toshiba, Hitachi, Fujitsu, ...

- **Grandis is focused on commercializing STT-RAM in 1–2 years**
  - It has the key fundamental and blocking patents in STT-RAM, and has early strategic partnerships in product development with key semiconductor memory players

- **Much progress has been made, but still plenty of room for innovation**
Thank You!

Please visit www.GrandisInc.com for more information