From Spin Torque Random Access Memory to Spintronic Memristor

Xiaobin Wang
Seagate Technology
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  dynamics characterization, device scale down challenges and opportunities

• Spin Torque Memristor:
  concept, device and application examples
Spin Torque Random Access Memory (SPRAM) Working Principle

Integrate magnetic tunneling junction (MTJ) with CMOS
Reading through magneto-resistance principle
Writing through spin torque excitation
SPRAM Switching Behavior

MTJ static picture

Dynamic MTJ switching vs static MTJ switching
- Black: Considering MTJ and CMOS coupling
- Blue: Switching without coupling to CMOS using $R_L$
- Red: Switching without coupling to CMOS using $R_{AP}$


MTJ switching asymmetry
- Spin torque switching asymmetry for a field balanced MTJ stack

**SPRAM System Dynamical Approach:**

**Quantum-Micromagnetic-SPICE**

- **Dynamical approach**
  - Macroscopic magnetic (size, Ms, etc)
  - MTJ electronic spin transport (band structure, tunneling)
  - CMOS I-V curve, equivalent capacitors, etc

**Dynamic CMOS circuit**

\[
I_M + I_{GD} = I_{DB} + I_T
\]

\[
I_{GD} = C_{GD} \cdot \left( \frac{dV}{dt} \right)
\]

\[
I_{DB} = C_{DB} \cdot \left( \frac{dV}{dt} \right)
\]

\[
I_M \cdot R(t) = V_{DD} - V \quad (BL \rightarrow SL) \text{ or}
\]

\[
I_M \cdot R(t) = -V \quad (SL \rightarrow BL)
\]


**Dynamic Magnetization**

Challenge for SPRAM to Scale Down

Field driving: switching field scales up with 1/volume or 1/surface dimension

Spin torque driving: switching current density scales up with 1/volume or 1/surface dimension

As magnetic device scales down, with CMOS driving strength decreasing, achieving fast nanosecond time scale magnetization switching and maintaining thermal stability at years time scale become a challenge.
Challenge for SPRAM to Scale Down

Spin torque MRAM device to device variations reduce sensing and writing margins.

As device scales down, increased variability is another challenge.
Current Reduction Through Magnetization Dynamics

Critical switching current \( \propto \frac{M_s^2 V \alpha}{\eta} \sqrt{(D_z - D_y)(D_z - D_x)} \)

\( D_x, D_y \) : demag factors in-plane, \( D_z \) : demag factor out-plane

Stable energy in equilibrium : \( M_s^2 V (D_y - D_x) \)

\( D_z \gg D_x, D_y \), different scaling behavior of MTJ writing current magnitude and thermal stability energy

Road leads to same scaling of switching current and thermal stability energy

Geometric wise: thin film for TMR etc.
Magnetization dynamics wise: Symmetric magnetization motion: \( D_z = D_y \)

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Current Reduction Through Magnetization Dynamics

RF frequency time varying polarization angle

- Constant polarization direction solution
- Optimal time varying polarization direction solution

Composite material stack

- Hard magnetic layer to keep thermal stability
- Soft magnetic layer to decrease switching field/current magnitude

Normalized magnetization $M_z/M_s$ vs. Time (sec)

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Current Reduction Through Electronic and Spin Transport Across Interface

Increase insulating layer thickness only, RA increases 5 times, critical switching voltage only increases 2.5 times

MTJ with spin moment conservation layer between free layer and top cap layer


Dual tunneling barrier, critical switching current down to 0.6MA/cm², quantum confinement effects?

Variation Controlling at Device Level

Unique Device characters leads to new sensing scheme

Self-reference sensing


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Variation Controlling at System Level

Reduce switching current requirement by intentionally move away from worst case scenario design

a smaller-than-worst-case transistor sizing approach. For 256Mb SPRAM design at 45nm node, under a normalized write current threshold deviation of 20%, the overall memory die size can be reduced by more than 20% compared with the conventional worst-case transistor sizing design.

Heat Asssited Solutions

Surface anti-ferromagnetic coupled (AFC) magnetic layer with relatively low Curier temperature:
At room temperature, the AFC coupling provides surface anisotropy to maintain thermal stability of the square magnetic element.
During the writing process, the joule heating of spin torque current raises temperature of AFC surface magnetic layer above Curier temperature and the AFC induced surface anisotropy disappears. The element can be switched at low threshold current.

Write current decreases with decreasing memory element dimension D. Meanwhile, the MTJ resistance increases with decreasing memory element dimension. For a given technology node, an optimal memory cell size can be found due to the tradeoff between critical switching current and MTJ resistance.

MTJ Memristor and Mutibit Data Storage and Logic

From nonlinear resistor point of view:

reversible branch: 11 to 10, 00 to 01

Irreversible branch: 00 to 10

From memristor point of view:

Switching from 00 to 10 and from 00 to 01 are all possible by adjusting pulse width

Different slope, switching depends upon integration of current, not current magnitude!
Memristor as Fourth Circuit Element

What makes memristor different from an ordinary constant resistor or even a current or voltage dependent nonlinear resistor: memristance is a function of charge, which depends upon the hysteretic behavior of the current (or voltage) profile.

Chua (1971) proposed memristor for logic completeness of circuit element

What makes memristor different from a capacitor or inductor is the ability to accumulate current or voltage information at constant voltage or current.

Memristance in Resistive Memory Stack

low resistance state

high resistance state

measured

1) Nano-scale two terminal device as two connecting resistors (doped region and undoped region)
2) Bias electric current drives the front of the doped region

Spintronic Memristor Through Spin Torque Induced Magnetization Motion

Spin Torque device: current electronic spin changes the magnetization state of the device. The magnetization state of the device depends upon the cumulative effects of electron spin excitations.

GMR/TMR device: resistance depends upon magnetization state

Spintronic memristor: resistance depends upon the integral effects of its current profile.

Domain Wall Memristor and Temperature Sensor

interactions between macroscopic coherent magnetic structures and random fluctuations

Nano-scale feature size, low cost, and mature integration technology with the CMOS process.

Targeting the highly integrated on-chip thermal detection applications

Memristor for Power Management

The ability to accumulate current/voltage through constant current and/or voltage driving strength: power monitor device

\[ E = \int VIdt = V \int Idt \]

Negative feedback: power control device


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Memristor for Data Security

Question: Administrator and user. Design a scheme to fight against following action: after reading the stored data information, the user tries to restore the device state to the same state as before reading, so that administrator could not find whether the data has been accessed.

Solution depends upon whether the user is given the limited or the same authority on device writing and reading compared to that of the administrator. For the case of user with limited reading and/or writing authority, data information security task can be achieved more easily. For limited writing authority case, user may not be able to restore the device to the state set by the administrator before. For reading limited case, the user may not know the state of the device set by the administrator.

A solution giving user and administrator the same authority on reading and writing:

1) Writing process: administrator sets high resistance state (0) fully saturated and low resistance state (1) partially saturated.

2) Reading process: two constant voltage pulses excite device a few times (order of 10). One pulse pushes domain wall toward high resistance end and the other pulse tries to push domain wall toward low resistance end.

3) The device reports two values for reading: 1) final state of the device close to high or low resistance state (High or Low) and 2) whether the device resistance has been significantly changed during reading (Yes or No).

Ref. X. Wang, Y. Chen,
Path to Future: Potentials

GMR with spin valve structure

TMR with tunneling structure

Physics process is clear and scaling behavior is well understood: controllable and tunable device

Easily integration on top of CMOS

New geometry structures

Spin blockade, half-metallic material

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Path to Future……

nano-scale, ultra-fast…….

variability, memory effects…….

analogue/digit mixture fuzzy, neural system

……

deterministic, precise digital control

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