Spin Electronics

Write Error Rate Slopes of In-Plane Magnetic Tunnel Junctions

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Abstract—Understanding bit error rates of magnetic tunnel junctions (MTJs) is critical for designing reliable spin-transfer-torque magnetoresistive random access memory. In this letter, we study the write error rate (WER) of two types of in-plane MTJs with the same film stacks except for the free layer and the capping layer. By comparative analysis of these two MTJ splits that show significantly different WER characteristics, we find that reducing average switching voltages does not necessarily improve WER slopes, resulting in decreased write margins for a sufficiently low WER requirement. Various magnetic measurements suggest that WER slopes and slope asymmetries are more strongly correlated to spin torque efficiencies rather than thermal stability factors.

Index Terms—Spin electronics, magnetic tunnel junction (MTJ), switching current asymmetry, bit error rate, thermal stability.

I. INTRODUCTION

To achieve reliable spin-transfer-torque magnetoresistive random access memory (STT-MRAM), it is crucial to understand the nature of bit error rates of magnetic tunnel junctions (MTJs). There are three basic mechanisms that contribute to bit error rates of STT-MRAM: thermal disturbance, read disturbance, and probabilistic write failure.

The thermal disturbance rate (TDR) of an MTJ array is directly correlated to static data retention and can be characterized by counting the number of bits exhibiting data retention failure after exposing STT-MRAM chips to elevated temperatures. To first order, the TDR of a single MTJ is governed by the energy barrier E_{B} between the two stable states. The probability P_{TD} of thermal disturbance after time t is typically estimated by the Néel–Brown relaxation time formula [Brown 1963]

$$P_{\mathrm{TD}} = 1 - \exp\left(-\frac{t}{\tau}\right), \qquad \tau = \tau_0 \exp\left(\frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T}\right) \tag{1}$$

where τ is the relaxation time constant, and τ_0 is the attempt period, commonly assumed to be 1 ns. Since thermal disturbance events in an MTJ array are dominated by bits in the tail of the E_{B} distribution with relatively small E_{B}, it is critical to improve the size uniformity of MTJ devices and reduce H_k variations to tighten the E_{B} distribution.

In the thermally activated STT switching regime, the switching probability of an MTJ device is described by [Li 2004]

$$P_{\mathrm{sw}} = 1 - \exp\left[\frac{t_p}{\tau_0}\exp\left(-\frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T}\left(1 - \frac{V}{V_{c0}}\right)\right)\right] \tag{2}$$

where t_p is the effective read pulse width, V is the applied voltage, and V_{c0} is the critical switching voltage. In the low-voltage read regime, the read disturbance rate (RDR) can be estimated by performing a Taylor expansion of (2) [Heindl 2011]

$$\ln(\mathrm{RDR}) = \ln\left(\frac{t_p}{\tau_0}\right) - \frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T}\left(1 - \frac{V}{V_{c0}}\right). \tag{3}$$

Equation (3) shows that E_{B} and V_{c0} can be extracted by measuring the RDR as a function of V and fitting the linear portion of ln(RDR). The validity of (3) has been experimentally verified [Driskill-Smith 2010, Heindl 2011], revealing that the slope of an ln(RDR) versus V plot is indeed linear. At chip level, t_p and V for read operations are typically predetermined to meet a set of overall circuit specifications. For reliable high-speed read operations ($t_p < 10$ ns), it is desirable to increase the read current. However, V_{c0} is directly correlated to write energy and tends to decrease as advances are made in MTJ materials research. To offset these decreases in V_{c0}, it is critical to enhance E_{B} to ensure sufficiently low RDR.

While (3) provides an estimation of RDR, it fails to predict the write error rate (WER) at sufficiently high voltages. For t_p of 50–100 ns, it has been reported that the WER follows a Gaussian cumulative distribution function (CDF) [Min 2010]. Above 500 ns, WER tends to fall off faster and can be fitted better with a Weibull CDF [Tang 2010]. Since the maximum allowable write voltage across an MTJ device is limited by time-dependent dielectric breakdown of the MgO barrier, it is important to obtain steep WER slopes. Recently, Butler and coworkers modeled the WER of perpendicular MTJs [Butler 2012], showing that the WER decays as $\exp[-(I/I_{c0}-1)\alpha\omega_0 t_p]$ for the applied current I much larger than the critical switching current I_{c0}. Here, α is the damping constant and ω_0 is the precession frequency.

To experimentally investigate the dominant factors that affect the WER slope, two types of in-plane MTJs (hereafter MTJ1 and MTJ2) fully integrated into a 45-nm CMOS logic platform, were examined to check correlations between various device parameters and WER. The nominal MTJ size was 40 nm $\times$ 110 nm. MTJ1 and MTJ2 have the same film stacks except for the free layer and capping layer. CoFeB-based free layers were used for both MTJs, but the capping layer of MTJ2 was

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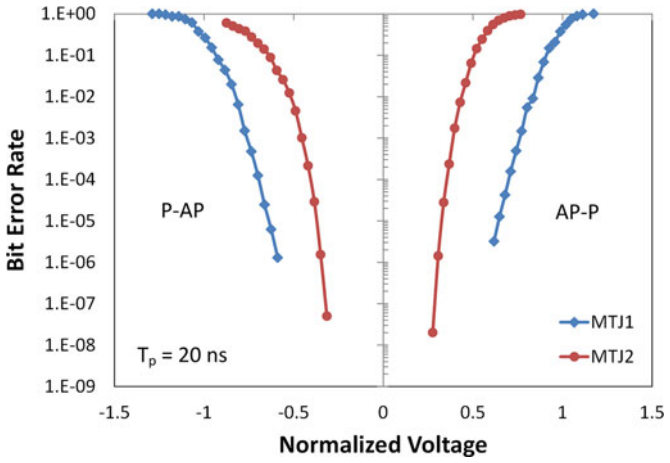

Fig. 1. RDRs of two representative MTJ devices with different free/capping layers. The pulse width is 20 ns.

optimized to lower V_{c0} while maintaining or enhancing E_B. The detailed stack structure is not disclosed due to proprietary information. The parallel-state resistance R_p values were comparable but MTJ2 showed higher tunneling magneto-resistance (150%) than MTJ1 (132%). For both MTJs, the average offset fields measured from resistance-field loops were nearly zero. Details about fabrication of the in-plane MTJs were reported earlier [Lee 2009]. The RDR and WER characteristics were measured from more than 30 MTJs of each type. MTJ2 showed distinctively degraded WER slopes for parallel-to-antiparallel (P-AP) switching, which resulted in asymmetric WER characteristics. In this paper, we discuss the implication of asymmetric WER on write margins and the origin of this asymmetry in conjunction with MTJ device parameters.

II. BIT ERROR RATE CHARACTERISTICS

Fig. 1 shows the RDR characteristics measured from a representative device of each type. The applied voltage was normalized to average switching voltage V_{c50} of MTJ1 measured at 20 ns. This normalization method is applied to all the relevant figures to highlight the difference between MTJ1 and MTJ2. MTJ2 shows steeper RDR slopes and reduced switching voltages, indicating increased E_B and decreased J_{c50} in comparison to MTJ1. Using (3), average E_B values extracted from RDR data were 41 k_BT for MTJ1 and 50 k_BT for MTJ2. The corresponding average V_{c0} values were 0.59 V for MTJ1 and 0.35 V for MTJ2.

Fig. 2 shows the corresponding WER characteristics (normal quantile plots). When the WER is less than 50%, WER data measured at 20–100 ns followed the Gaussian CDF for all the MTJs measured. As the pulse width decreases, WER slopes (units of sigma/V) decrease for both MTJ1 and MTJ2, but this trend is more pronounced for MTJ2. It is also noteworthy that MTJ2 shows considerably asymmetric WER slopes [see Fig. 2(b)]. This asymmetry is aggravated as the pulse width decreases.

To verify that this trend does not result from bit-to-bit variations, the average WER characteristics of all the measured

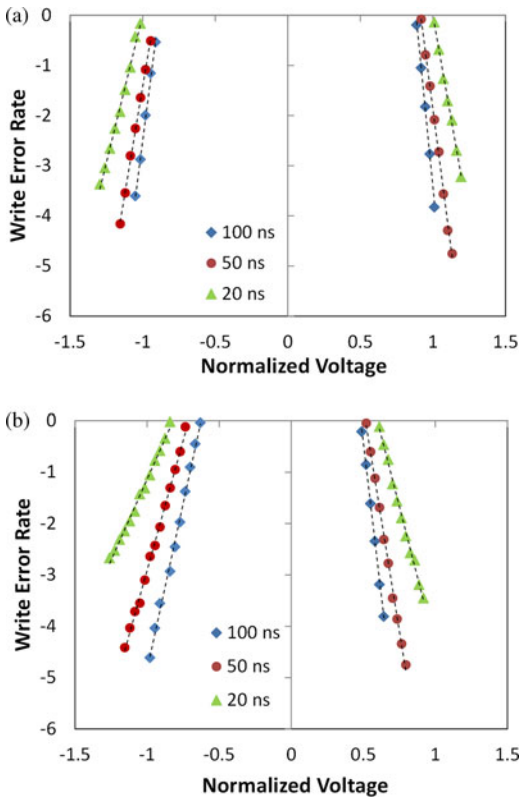

Fig. 2. Normal quantile plots of WERs measured from two representative MTJ devices. (a) MTJ1. (b) MTJ2. Only MTJ2 shows asymmetric WER slopes. Dotted lines are fits to the Gaussian CDF.

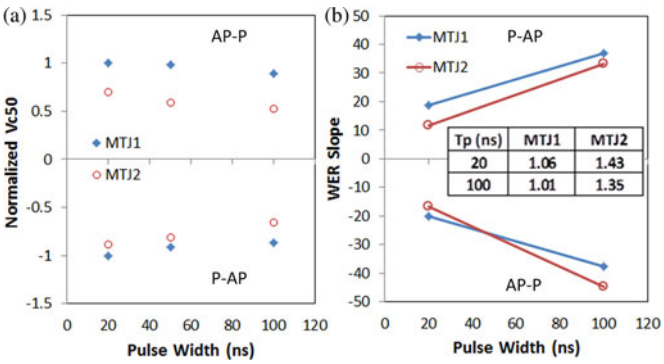

Fig. 3. (a) Normalized V_{c50} versus pulse width. (b) WER slopes versus pulse width. The data points averaged from >30 MTJs per split. The inset shows WER asymmetry of each split.

MTJs were examined at 20 and 100 ns. Fig. 3(a) shows that V_{c50} of MTJ2 is smaller than those of MTJ1 at 20–100 ns. The difference is greater in AP-P switching (positive voltage) than P-AP switching (negative voltage) due to relatively large switching current asymmetry of MTJ2. The switching current asymmetry, defined as the ratio of 50% P-AP to AP-P switching currents, was 1.2 for MTJ1 and 1.8 for MTJ2. Though MTJ2 demonstrates improved MTJ performance metrics, the WER slopes behave quite differently, as shown in Fig. 3(b). At 100 ns, MTJ2 shows steeper WER slope than MTJ1 for AP-P switching, but not for P-AP switching. At 20 ns, both AP-P and P-AP WER slopes of MTJ2 are worse than those of MTJ1. The table inset in Fig. 3(b)

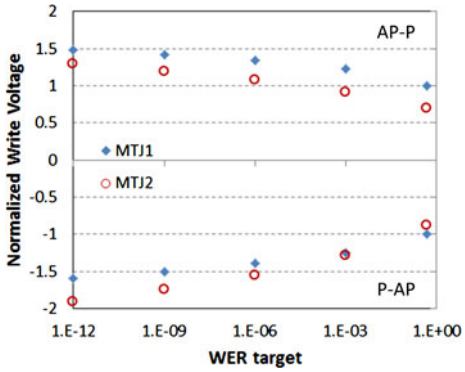

Fig. 4. Write voltage requirement versus WER targets. The write voltage requirement was estimated from the Gaussian CDF fits. This is the average behavior of all the measured MTJs.

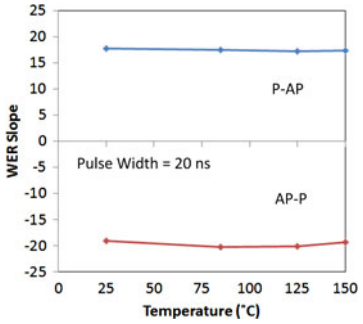

Fig. 5. WER slopes as a function of temperature.

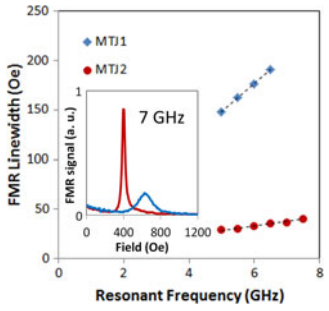

Fig. 6. FMR linewidth versus resonant frequency. The damping constant values of MTJ1 and MTJ2 were 0.007 and 0.037, respectively. The inset shows the FMR peaks measured at 7 GHz.

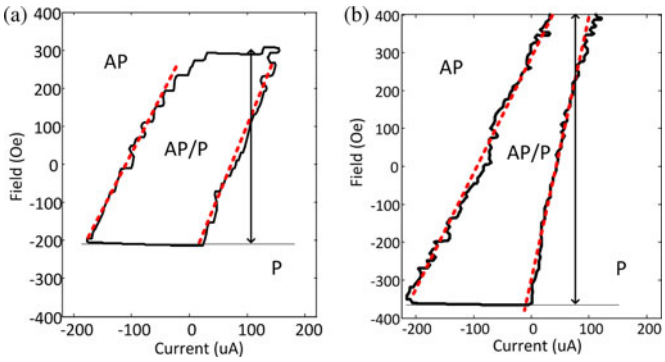

Fig. 7. SSDs of (a) MTJ1 and (b) MTJ2. MTJ2 shows substantially different slopes between AP-P and P-AP switching boundaries, as indicated by dotted lines.

shows the asymmetry of WER slopes (hereafter WER asymmetry), defined as the ratio of P-AP to AP-P WER slopes. While MTJ1 shows WER asymmetry ~1 at both 100 and 20 ns, MTJ2 exhibits considerably larger WER asymmetry.

To illustrate the impact of the WER asymmetry on write margins, write voltage requirements were estimated by extrapolating the Gaussian fits for varying WER targets at 20 ns (see Fig. 4). Although low-probability bifurcated switching and WER ballooning have been reported [Min 2010], no such ballooning was observed for the measured MTJ devices. This is essential to perform the extrapolation and estimate the write margin. For the AP-P switching direction, MTJ2 requires less voltage because of significantly reduced V_{c50}. For P-AP switching, the write voltage requirement is dominated by WER slopes. At high WER targets, MTJ2 provides better margins but this advantage is quickly lost as soon as the WER target becomes lower than 0.1%. This result reveals that WER slopes need to be examined as separate MTJ device parameters to check actual write margins for a given WER target.

III. ORIGIN OF WER ASYMMETRY

Despite having smaller E_B, MTJ1 showed steeper WER slopes than MTJ2. This indicates that E_B may not be the dominant factor that determines WER slopes. To verify this, the WER slopes of representative MTJs were examined at various temperatures. Fig. 5 shows that the WER slopes measured at 20 ns are insensitive to temperature up to 150 °C. Similar results were also observed at 100 ns.

To investigate material parameters that can affect WER slopes, we examined the corresponding blanket films of MTJ1 and MTJ2. For in-plane MTJs, the intrinsic critical switching current density J_{c0} is given by [Slonczewski 1996]

$$J_{c0} = \frac{2e}{\hbar}\frac{\alpha}{\eta}M_s t\left(H_{ext} + H_k + \frac{H_d}{2}\right) \quad (4)$$

where η is the spin torque efficiency, M_s is the saturation magnetization, t is the free layer thickness, H_{ext} is the external field, H_k is the uniaxial anisotropy field, and H_d is the effective demagnetization field. First, minor loops of full-stack MTJ films were measured by vibrating sample magnetometer (VSM). The free layers of MTJ1 and MTJ2 showed comparable $M_s t$ values. Next, α and H_d were extracted using ferromagnetic resonance (FMR) measurements [Beaujour 2007]. Fig. 6 shows FMR linewidth versus resonant frequency. Since the intrinsic damping constant is proportional to the slope of this plot [Beaujour 2007], this result reveals that MTJ2 has significantly smaller damping constant (~0.007) than MTJ1 (~0.037). The extracted damping constant of MTJ2 is close to that of bulk CoFeB. On the other hand, MTJ1 and MTJ2 showed comparable H_d values (~5 kOe).

To assess η and H_k qualitatively, we also performed switching state diagram (SSD) measurements. For a given field bias, dc currents were swept to generate these maps of R(H,I) space. Fig. 7 shows the SSD plots of two representative MTJ devices

from MTJ1 and MTJ2 splits. Two SSD plots are distinctively different in terms of the height of the bistable regions (indicated by solid arrows) and slopes in AP-P and P-AP switching boundaries (indicated by dotted lines). In a macrospin approximation, the Landau–Lifshitz–Gilbert equation predicts that the height is directly correlated to H_k at 0 K [Stiles 2006]. Hence, H_k of MTJ2 should be greater than that of MTJ1. This explains why MTJ2 consistently shows enhanced E_B over MTJ1.

So far, we have examined all the parameters in (4) except for η, but none of them explains the reduced WER slopes in MTJ2. In the original framework of Slonczewski's STT model that considers only in-plane spin torques, η was considered to be a function of spin polarization [Diao 2005]. However, there are other factors that can affect η, including out-of-plane spin torques [Kubota 2008, Sankey 2008] and electric-field-induced anisotropy [Maruyama 2009, Wang 2011]. η is not a directly measurable quantity; hence, we examine this factor qualitatively using the SSD technique. The slopes of AP-P and P-AP switching boundaries are approximately proportional to $\eta/(\alpha M_s t)$ [Stiles 2006]. Since $\alpha M_s t$ is the same for AP-P and P-AP switching, the slope difference indicate an asymmetry in η. If we assume equal η values, MTJ2 is expected to show steeper switching boundary slopes than MTJ1 because MTJ2 has smaller α while maintaining comparable $M_s t$. However, MTJ2 shows a steeper boundary only for AP-P switching, indicating considerably lower η for P-AP switching. Therefore, it is suggested that asymmetric η affects WER slopes and causes WER asymmetries.

IV. CONCLUSION

MTJ devices are typically optimized to have lower average switching current density J_{c50} and higher E_B. As a result, J_{c50}/E_B has been used as a figure of merit. However, our results showed that reducing J_{c50} does not necessarily guarantee increased write margins for a given WER target when considering WER slopes. In particular, the WER slopes for AP-P and P-AP switching can show significant asymmetry at relatively short write pulse widths. This implies that the WER slope has to be considered as a separate device parameter particularly for high-speed STT-MRAM. To identify the origin of WER asymmetry, we performed VSM, FMR, and SSD measurements. The results indicate that spin torque efficiency can affect WER slopes and is responsible for WER asymmetry.

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