

Joint Stochastic Decoding of LDPC Codes and Partial-Response Channels

Saeed Sharifi Tehrani[†], Paul H. Siegel[‡], Shie Mannor[§] and Warren J. Gross[◇]

[†]*Micron Technology, Inc., San Diego, CA*

[‡]*Center for Magnetic Recording Research, University of California, San Diego, CA*

[§]*Dept. of Electrical Engineering, Technion-Israel Institute of Technology, Haifa, Israel*

[◇]*Dept. of Electrical and Computer Engineering, McGill University, Montreal, QC, Canada*

E-mail: ssharifi@ieee.org, psiegel@ucsd.edu, shie@ee.technion.ac.il, warren.gross@mcgill.ca

Abstract—This paper proposes the application of the stochastic decoding approach for joint decoding of Low-Density Parity-Check (LDPC) codes and Partial-Response (PR) channels. It shows how the computationally-intensive operations required in the PR channel detection can be performed using simple circuitry in the stochastic domain. Performance results of the stochastic approach are compared against conventional joint decoders with fixed-point and floating-point precisions.

Keywords—Stochastic decoding, low-density parity-check codes, partial-response channels.

I. INTRODUCTION

Magnetic recording systems, primarily hard disks, are widely used in today’s storage solutions. It is known that at high bit densities, magnetic recording systems must cope with the inter-symbol interference (ISI). Partial response (PR) channels are discrete channels that characterize the unequalized ISI and are used to model magnetic recording channels. The idea of applying a (bit-based) message-passing detector/decoder matched to the combination of a PR channel and an LDPC code was proposed in [1]. In this scheme, the PR channel detector and the LDPC decoder operate on two separate bipartite graphs and iteratively exchange their information in a turbo-like fashion (see Fig. 2(a)). Bit-based message-passing graphs of some PR channels have many short cycles that can cause high error-floors [1]. The error-floor phenomenon, however, was not observed in [2] for the case where powerful LDPC codes (with large block size) are used. Nevertheless, since the operations in the PR channel detection are complex, the joint decoding approach has not been attractive for hardware implementations.

Stochastic decoding [3], [4] is a new approach for iterative decoding on graphs. In stochastic decoding, instead of propagating probabilistic beliefs by exchanging distinct probability messages, as in conventional message-passing algorithms, beliefs are conveyed in streams of stochastic bits in a sense that the probability of observing a 1 in a bit stream is equal to the original (encoded) probability. This representation results in low hardware-complexity processing nodes that perform computationally-intensive operations [5]. However, stochastic decoding is prone to the acute problem of latching [4]. This problem is caused by correlated bit streams

within cycles in the code’s factor graph, and significantly deteriorates the performance of stochastic decoders. Edge memories [4], [6], Tracking Forecast Memories (TFMs) [7], and Majority-based Tracking Forecast Memories (MTFMs) [8] are first solutions proposed to address the acute problem of latching in practical LDPC decoders. These “rerandomization” units efficiently extract the evolving statistics of stochastic bit streams and rerandomize them to disrupt latching. FPGA and ASIC implementations of practical stochastic LDPC decoders have been recently reported in [6]–[8]. It has been shown that stochastic decoders can deliver good decoding performance and high throughput while having low silicon area consumption. For instance, the (2048,1723) fully parallel stochastic LDPC decoder in [8] occupies a silicon core area of 6.38 mm² in CMOS 90 nm technology, achieves a maximum clock frequency of 500 MHz, and provides a maximum throughput of 61.3 Gb/s. This decoder exhibits good error-correcting behavior down to a bit-error-rate (BER) of about 4×10^{-13} .

In this paper, we propose the application of the stochastic decoding approach for joint decoding of LDPC codes and PR channels. We show how the complex operations in PR channel detectors can be performed using simple circuitry in the stochastic domain. We demonstrate the performance of this approach and discuss its latency and throughput tradeoffs.

II. OVERVIEW

Fig. 1 depicts the system model used in [1] and this paper. In this model, an independent and identically distributed binary vector $\mathbf{x} = (x_1, \dots, x_n)$, where $x_i \in \{0, 1\}$, is passed through a PR channel. The transfer polynomial of the PR channel is $h(D) = \sum_{j=0}^d h_j D^j$, where d is the channel degree, and h_j is a real number. The output vector of the PR channel is $\mathbf{y} = (y_1, \dots, y_{n+d})$, and its output alphabet set is A , where $y_i \in A$. The vector \mathbf{y} is passed through an AWGN channel with zero mean and a single-sided noise power spectral density of N_0 . The joint decoder receives the vector $\mathbf{r} = (r_1, \dots, r_{n+d})$ from the AWGN channel. Similar to [1], we consider two types of PR channels: the dicode channel and the EPR4 channel. The transfer polynomial of the dicode channel is $h(D) = 1 - D$. In the dicode channel,



Figure 1. System model.

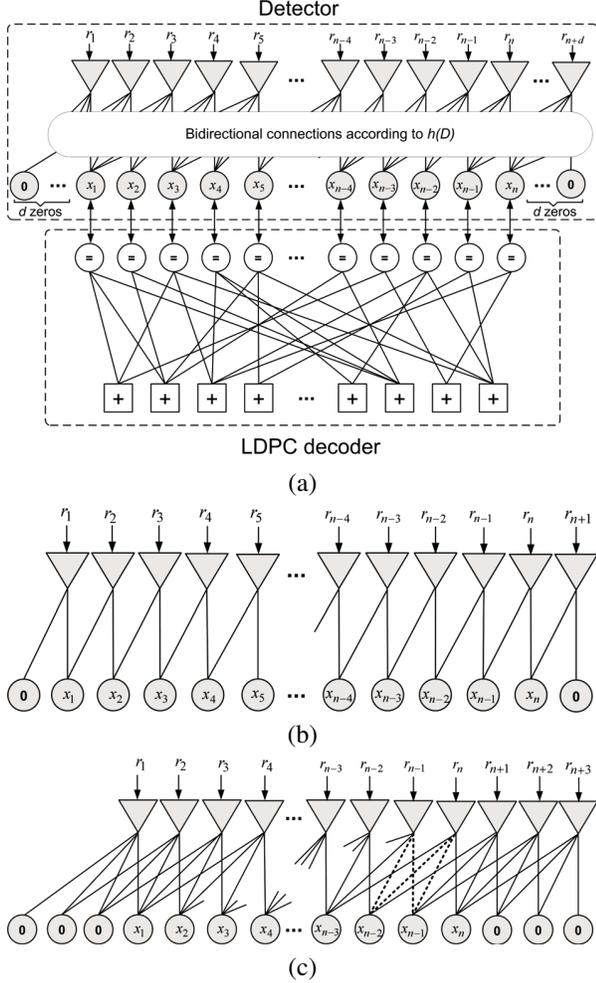


Figure 2. (a) Joint message-passing diagram for decoding LDPC codes and PR channels. d is the degree of the PR channel. (b) The message-passing diagram for the dicode channel and (c) the EPR4 channel in which a length-4 cycle is highlighted.

$d = 1$ and $A = \{-1, 0, +1\}$. The EPR4 channel model is a practical PR channel model considered in magnetic recording applications. In this channel, $h(D) = 1 + D - D^2 - D^3$, $d = 3$, and $A = \{-2, -1, 0, +1, +2\}$. We assume that the PR model starts from the zero state, and it is terminated at the zero state.

Fig. 2(a) depicts the block diagram of the joint message-passing decoding of LDPC codes and PR channels as proposed in [1], [9]. The joint message-passing decoder is comprised of a PR channel detector and an LDPC decoder.

Similar to LDPC codes, the message-passing detector for the PR channel detector is represented by a bipartite graph. This graph has two types of nodes: triangle nodes which receive the noisy samples, r_i , from the AWGN channel, and bit nodes. In Fig. 2(a), triangle nodes are depicted as grey triangles and bit nodes are depicted as grey circles. The connection between triangle nodes and bit nodes is determined by $h(D)$, i.e., a triangle node is connected to a bit node if and only if $h(D)$ indicates a direct dependence between the input and the corresponding output of the PR channel. The detector operates for T iterations on the received samples from the channel, then it passes its soft outputs to the LDPC decoder. The LDPC decoder runs for S iterations and its soft outputs are passed back to the detector. This scheme is repeated for U global/turbo iterations [1], [9]. Figs. 2(b) and (c) show the message-passing graph for the dicode and the EPR4 channels. Note that the graph for the dicode channel is acyclic, but the graph for the EPR4 channel has many length-4 cycles.

A. Operation of Triangle Nodes and Bit Nodes

Triangle nodes and bit nodes in the detector exchange probability messages that represent $\Pr(x_i = 1)$. Their outgoing messages are produced according to the Sum-Product Algorithm (SPA) rule, in which the outgoing message for an edge is based on all incoming messages, excluding the message received from that edge. Let $\mathbf{x}_{p-d}^p = (x_{p-d}, \dots, x_p)$ and let $\mathbf{x}_{p-d}^{p \setminus m}$ be a vector for the same bits excluding bit x_m for $p-d \leq m \leq p$. Let $\mathbf{b}_0^{d \setminus m-p+d} = (b_0, \dots, b_d)$ be a vector of binary inputs to the PR channel except for b_{m-p+d} , and let $B_{m,p,d}$ be the set of all such binary inputs. The probability message from the p -th triangle node to the m -th bit node is $R_{pm}(1)$, and the message from the m -th bit node to the p -th triangle node is $Q_{mp}(1)$. $R_{pm}(\cdot)$ and $Q_{mp}(\cdot)$ are defined as functions of j , where $j \in \{0, 1\}$. The p -th triangle node computes $R_{pm}(j)$ as follows [1], [9]:

$$\begin{aligned}
 R_{pm}(j) &= \Pr(x_m = j | r_p) = \\
 &= \sum_{a \in A, \mathbf{b}_0^{d \setminus m-p+d} \in B_{m,p,d}} \Pr(x_m = j, \mathbf{x}_{p-d}^{p \setminus m} = \mathbf{b}_0^{d \setminus m-p+d}, y_p = a | r_p) \\
 &= \sum_{a \in A, \mathbf{b}_0^{d \setminus m-p+d} \in B_{m,p,d}} \Pr(x_m = j, \mathbf{x}_{p-d}^{p \setminus m} = \mathbf{b}_0^{d \setminus m-p+d}, y_p = a) \times \\
 &= \frac{\Pr(r_p | y_p = a) \Pr(y_p = a | \mathbf{x}_{p-d}^{p \setminus m} = \mathbf{b}_0^{d \setminus m-p+d}) \prod_{u=p-d}^{p \setminus m} Q_{up}(b_{u-p+d})}{\Pr(r_p)}. \tag{1}
 \end{aligned}$$

In the above equation, the term $\Pr(x_m = j, \mathbf{x}_{p-d}^{p \setminus m} = \mathbf{b}_0^{d \setminus m-p+d}, y_p = a)$ is either zero or one, and the term $\Pr(y_p = a | \mathbf{x}_{p-d}^{p \setminus m})$ is equal to 0.5 for all nonzero terms in the summation. Also, the term $\Pr(r_p | y_p = a)$ is the channel probability, which is calculated using the knowledge that the channel is AWGN. Finally, $\Pr(x_m = j, \mathbf{x}_{p-d}^{p \setminus m} =$

$b_0^{d \setminus m-p+d}, y_p = a$) are the prior probabilities which are factored into individual probability messages sent by the connected bit nodes to the p -th triangle node [1], [9].

The operation of bit nodes is the same as the operation of variable nodes (VNs) in the SPA. The m -th bit node computes its outgoing message for the p -th triangle node, $Q_{mp}(j)$, as follows [1], [9]:

$$\begin{aligned}
 Q_{mp}(j) &= \frac{\prod_{u=m}^{m+d \setminus p} \Pr(x_m = j | r_u)}{\prod_{u=m}^{m+d \setminus p} \Pr(x_m = 1 | r_u) + \prod_{u=m}^{m+d \setminus p} \Pr(x_m = 0 | r_u)} \\
 &= \frac{\prod_{u=m}^{m+d \setminus p} R_{um}(j)}{\prod_{u=m}^{m+d \setminus p} R_{um}(1) + \prod_{u=m}^{m+d \setminus p} R_{um}(0)}. \tag{2}
 \end{aligned}$$

III. THE PROPOSED METHOD

The triangle node operation in the joint message-passing decoding is a computationally-intensive operation which requires the division, multiplication, and summation of probabilities. It is possible to perform this operation in the log-domain to avoid division and multiplication, but even by using the log transformation, the triangle node's operation requires the evaluation of complex nonlinear functions (see [2]). In this section, we propose hardware architectures that perform the triangle node operation for the dicode and the EPR4 channels using the stochastic approach. Because the operation of bit nodes in a message-passing channel detector is the same as VNs in a LDPC decoder, stochastic VNs discussed in our previous publications (e.g., [7], [8]) can be used to perform bit node operations in a stochastic PR channel detector. In this regard, we do not discuss the hardware architectures of stochastic bit nodes in this paper.

In joint stochastic decoding, channel probabilities, $\Pr(r_p | y_p \in A)$, are transformed into stochastic bit streams. Similar to stochastic LDPC decoding, this transformation is done by comparing each channel probability to a (pseudo) random number that changes in every decoding cycle. The output bit stream of the comparator represents the corresponding channel probability [4], [6]–[8]. In the dicode channel, the alphabet set A has three elements; therefore, each triangle node transforms three channel probabilities to stochastic streams, i.e., $\Pr(r_p | y_p = -1)$, $\Pr(r_p | y_p = 0)$, and $\Pr(r_p | y_p = +1)$. Similarly, in the EPR4 channel, A has five elements and each triangle node transforms five channel probabilities to stochastic streams, i.e., $\Pr(r_p | y_p = -2)$, $\Pr(r_p | y_p = -1)$, $\Pr(r_p | y_p = 0)$, $\Pr(r_p | y_p = +1)$, and $\Pr(r_p | y_p = +2)$.

Each triangle node in the stochastic detector receives one bit from each of its (channel) comparators in every decoding

cycle.¹The stochastic channel detector operates by stochastic triangle nodes and bit nodes exchanging bits for T_{SD} decoding cycles. The detector then passes its soft output (extracted by TFMs) to the stochastic LDPC decoder which runs for a maximum of S_{SD} decoding cycles. The stochastic LDPC decoder performs syndrome checking in every decoding cycle to terminate the joint decoding process as soon as all the parity-checks are satisfied. If this termination criterion is not satisfied within S_{SD} decoding cycles, the stochastic LDPC decoder passes back its soft outputs (extracted by TFMs [7]) to the channel detector. This scheme is repeated for at most U global/turbo iterations.

A. Stochastic Triangle Nodes for the Dicode Channel

As mentioned previously, the message-passing graph of the dicode channel is acyclic. In acyclic graphs, the latching problem does not hold [4]. In this respect, the proposed stochastic triangle node architecture for the dicode channel does not use rerandomization units such as TFMs [7] and MTFMs [8]. From (1), it follows that we can write $R_{pm}(1)$ in the form of

$$R_{pm}(1) = \frac{P_1}{P_1 + P_0}, \tag{3}$$

where, for the case of the dicode channel,

$$\begin{aligned}
 P_1 &= \Pr(x_p = 1, r_p) = 0.5 \times \Pr(r_p | y_p = +1)(1 - Q_{(m-1)p}) \\
 &\quad + 0.5 \times \Pr(r_p | y_p = 0)Q_{(m-1)p}, \tag{4}
 \end{aligned}$$

and $P_0 = \Pr(x_p = 0, r_p)$ is computed similarly from (1).

Fig. 3(a) depicts the proposed hardware architecture to compute $R_{pm}(1)$ in a stochastic triangle node for the dicode channel detector. A similar hardware architecture is used to compute $R_{p(m-1)}(1)$. In this architecture, the inverse operation on $Q_{(m-1)p}$ is performed using a NOT gate, and the multiplication of probabilities is performed using AND gates. The output of each AND gate in the figure forms a term for the summation in (4) to compute P_1 (and similarly to compute P_0). The stochastic summation [5] is performed by two 2-input OR gates. The output streams of the OR gates shown in the figure represent $P'_1 \approx 2P_1$ and $P'_0 \approx 2P_0$. Finally, the stochastic streams representing P'_1 and P'_0 are passed to a JK flip-flop that performs a division [3], [5] and its output bit stream represents $P'_1/(P'_1 + P'_0)$, which approximates $R_{pm}(1) = P_1/(P_0 + P_1)$.

The degree-2 bit nodes used in the stochastic dicode channel detector are based on basic stochastic VNs, where a JK flip-flop is used to perform division (see [3], [4] for details).

¹A decoding cycle (stochastic iteration) refers to the exchange of one bit between the two types of nodes in a bipartite message-passing graph.

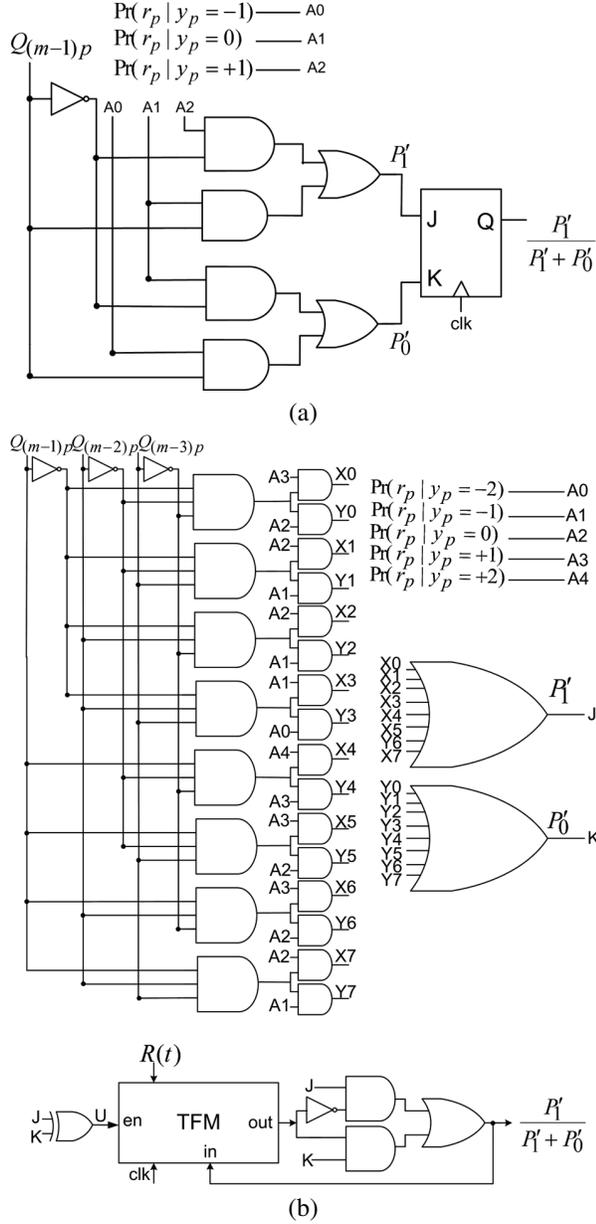


Figure 3. The hardware architecture of stochastic triangle node for (a) the dicoding channel and (b) the EPR4 channel (only one output and its corresponding inputs are shown). $R(t)$ is a (pseudo) random number varying in every decoding cycle.

B. Stochastic Triangle Nodes for the EPR4 Channel

The message-passing graph for the EPR4 channel has many length-4 cycles (see Fig. 2(c)). These short cycles severely intensify the latching problem in the stochastic channel detector and deteriorate the BER decoding performance of joint stochastic decoding. Moreover, triangle nodes and bit nodes in the EPR4 channel detector have higher node degrees and perform more complex operations compared to the triangle nodes and bit nodes in the dicoding channel.

In this respect, the proposed architecture for stochastic triangle nodes in the EPR4 channel detector relies on TFMs, as rerandomization units, to alleviate the latching problem [7], [8].

In the EPR4 channel, the term P_1 in (3) is computed as:

$$\begin{aligned}
 P_1 &= \Pr(x_p = 1, r_p) = 0.5 \times \\
 &\left(\Pr(r_p | y_p = +1)(1 - Q_{(m-1)p})(1 - Q_{(m-2)p})(1 - Q_{(m-3)p}) \right. \\
 &+ \Pr(r_p | y_p = 0)(1 - Q_{(m-1)p})(1 - Q_{(m-2)p})Q_{(m-3)p} \\
 &+ \Pr(r_p | y_p = 0)(1 - Q_{(m-1)p})Q_{(m-2)p}(1 - Q_{(m-3)p}) \\
 &+ \Pr(r_p | y_p = -1)(1 - Q_{(m-1)p})Q_{(m-2)p}Q_{(m-3)p} \\
 &+ \Pr(r_p | y_p = +2)Q_{(m-1)p}(1 - Q_{(m-2)p})(1 - Q_{(m-3)p}) \\
 &+ \Pr(r_p | y_p = +1)Q_{(m-1)p}(1 - Q_{(m-2)p})Q_{(m-3)p} \\
 &\left. + \Pr(r_p | y_p = 0)Q_{(m-1)p}Q_{(m-2)p}Q_{(m-3)p} \right). \tag{5}
 \end{aligned}$$

Also, $P_0 = \Pr(x_p = 0, r_p)$ is computed similarly from (1).

Fig. 3(b) depicts the proposed hardware architecture to compute $R_{pm}(1)$ in a stochastic triangle node for the EPR4 channel. Similar hardware architectures are used to compute $R_{p(m-1)}(1)$, $R_{p(m-2)}(1)$, and $R_{p(m-3)}(1)$. In the architecture shown, the network of AND gates computes the terms that are needed for summations in (5) to compute P_1 (and similarly P_0). The stochastic summation is performed by two 8-input OR gates. The output streams of the OR gates shown in the figure represent $P_1' \approx 2P_1$ and $P_0' \approx 2P_0$. The division required to compute $R_{pm}(1)$ in (3) is performed by a TFM-based stochastic divider. The operation and the update rule of the TFM-based divider is the same as a JK flip-flop divider, however, instead of a flip-flop, a TFM is used to efficiently rerandomize the output stochastic bit stream². The output stream of the TFM-based divider represents $P_1'/(P_1' + P_0') \approx 2P_1/(2P_1 + 2P_0) = P_1/(P_1 + P_0)$. In this divider, the TFM is updated when $J \neq K$. The output bit of the divider is 1 when $J = 1$ and $K = 0$, and it is 0 when $J = 0$ and $K = 1$. Also, when $J = K = 0$ the output bit of the TFM is directly used as the output of the divider (hold state), and when $J = K = 1$ the inverse of the output bit of the TFM is used as the output of the divider (reverse state).

The degree-4 bit nodes used in the stochastic EPR4 detector are based on the reduced-complexity MTFM-based stochastic VNs with $T_u = 4$ and $T_m = 2$ (see [8] for details).

IV. DECODING PERFORMANCE RESULTS

Fig. 4(a) shows the BER decoding performance of the stochastic approach for joint decoding of a (2000,1000)

²A TFM has about 350 gate count complexity when synthesized for maximum possible speed in CMOS 90nm technology [7].

LDPC code and the dicode PR channel.³For the sake of comparison, the figure also shows the decoding performance results obtained for the floating-point joint message-passing decoding (with a floating-point channel detector and a floating-point SPA-based LDPC decoder), and the dicode channel truncated union bound from [1], [10]. We used $U = 16$, $T = 3$, and $S = 3$ for the floating-point SPA-based message-passing decoding. Also, for joint stochastic decoding, we used $U = 16$, $T_{SD} = 100$ decoding cycles for detection, and $S_{SD} = 100$ decoding cycles for stochastic LDPC decoding. The (2000,1000) stochastic LDPC decoder used in joint decoding relies on TFMs with a relaxation coefficient of $\beta = 2^{-4}$. The LDPC decoder applies syndrome checking to terminate the joint decoding process as soon as all the parity-checks are satisfied. As shown, at a BER of about 10^{-8} , the proposed joint stochastic decoder is able to provide a decoding performance within 0.4 dB of the floating-point joint message-passing.

Fig. 4(b) shows the BER decoding performance of the stochastic approach for joint decoding of a (2000,1000) LDPC code and the EPR4 PR channel. Also shown in the figure are the decoding performance of floating-point joint message-passing decoding using a floating-point channel detector and a floating-point SPA-based LDPC decoder, and the EPR4 channel truncated union bound from [1], [10]. To show the effects of quantization in the EPR4 channel detector, the figure also depicts performance results for joint message-passing decoding using an 8-bit channel detector and a floating-point SPA-based LDPC decoder. We used $U = 16$, $T = 8$, and $S = 8$ in both joint message-passing decoding schemes. For joint stochastic decoding, we used $U = 16$, $T_{SD} = 200$ decoding cycles for detection, and $S_{SD} = 200$ decoding cycles for TFM-based stochastic LDPC decoding. Results demonstrate the applicability of the proposed stochastic approach for joint decoding of LDPC codes and the EPR4 channel. Despite the existence of a high number of length-4 cycles in the detector graph of the EPR4 channel, which severely intensify the latching problem, no error-floor is observed down to a BER of about 10^{-8} . Compared to the dicode channel, more decoding loss with respect to the floating-point joint message-passing is observed. A comparison of joint message-passing decoding with floating-point and 8-bit channel detectors reveals the sensitivity of the BER decoding performance to the number of quantization levels used in the EPR4 channel detector. The decoding performance of the joint stochastic decoding is within about 0.6 dB of the joint message-passing decoding with an 8-bit channel detector and a floating-point SPA-based LDPC decoder.

³The energy per bit is defined as $E_b = E_y/R$, where R is the rate of the LDPC code, and E_y is the average energy of y_i 's. E_y is calculated by considering the probabilities of occurrence of $y_i \in A$, given equiprobable channel inputs $x_i \in \{0, 1\}$.

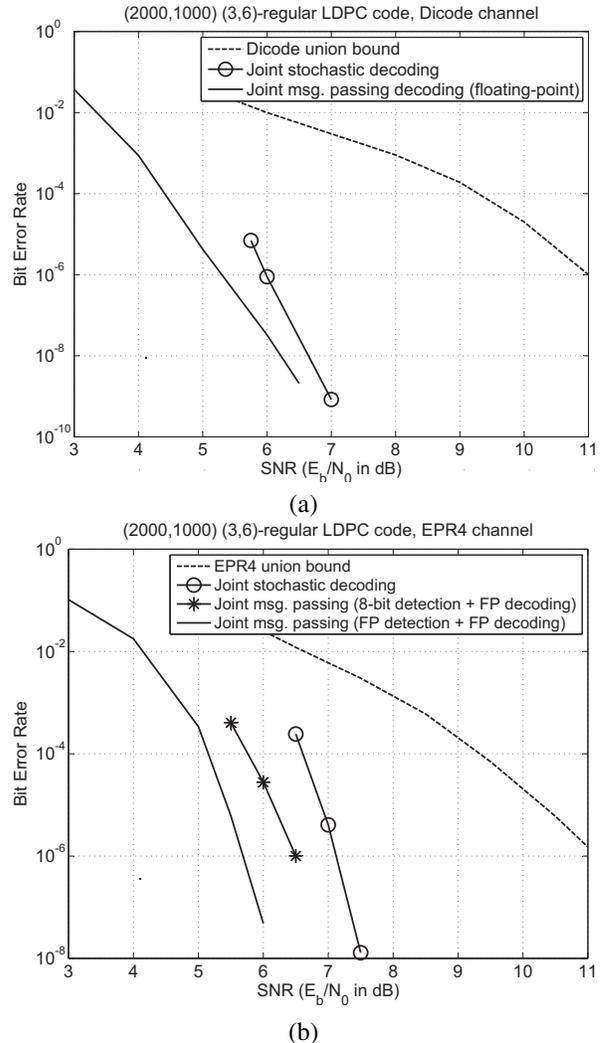


Figure 4. Results for joint decoding of a (2000,1000) LDPC code and (a) the dicode channel, (b) the EPR4 channel.

V. DECODING LATENCY AND THROUGHPUT

The ASIC implementations of stochastic LDPC decoders in our previous publications has shown that clock frequencies in the order of 500 MHz can be achieved for fully parallel ASIC stochastic LDPC decoders (in CMOS 90nm technology) (see [7], [8]). The decoding latency of the joint stochastic decoder is determined by $U(T_{SD} + S_{SD})$. For the dicode channel and the EPR4 channel, the decoding latencies are 3200 decoding cycles and 6400 decoding cycles, respectively, where each decoding cycle takes one clock cycle. Fig. 5 shows the decoding latency of the joint decoder for different clock frequencies ranging from 100 MHz to 500 MHz. It should be noted that magnetic recording applications have decoding latency requirements usually in the order of milliseconds. As shown, the decoding latency for the case of the dicode channel ranges from 0.0320

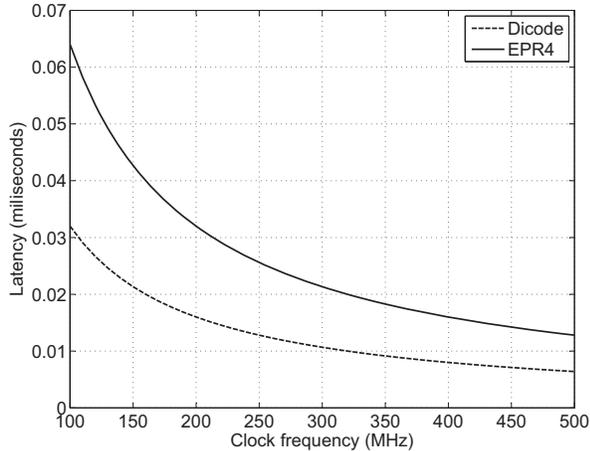


Figure 5. Estimated latency of joint stochastic decoding for different clock frequencies.

down to 0.0064 milliseconds, and for the case of the EPR4 channel, it ranges from 0.0640 down to 0.0128 milliseconds.

The throughput of the joint decoder is determined by the average number of decoding cycles used. This is because the stochastic LDPC decoder uses an early decoding termination criterion that stops the joint decoding process as soon as all the parity-checks are satisfied (see [7], [8]). Fig. 6 (a) depicts the average number of decoding cycles used for joint stochastic decoding at different SNRs for the dicode and the EPR4 channels. Also, Figs. 6(b) and (c) show the corresponding (core) throughput for different clock frequencies ranging from 100 MHz to 500 MHz. As shown, the average number of decoding cycles decreases significantly in low BER regimes (high E_b/N_0), which enables the joint stochastic decoder to provide multi-Gb/s throughput.

VI. CONCLUSION

This paper proposed the novel application of joint stochastic decoding of LDPC codes and PR channels that are considered in practical magnetic recording applications. It proposed low hardware-complexity architectures for stochastic triangle nodes to perform computationally-intensive operations required in the dicode and the EPR4 channel detectors. Results demonstrated the applicability of the stochastic approach for joint decoding of LDPC codes and practical PR channels.

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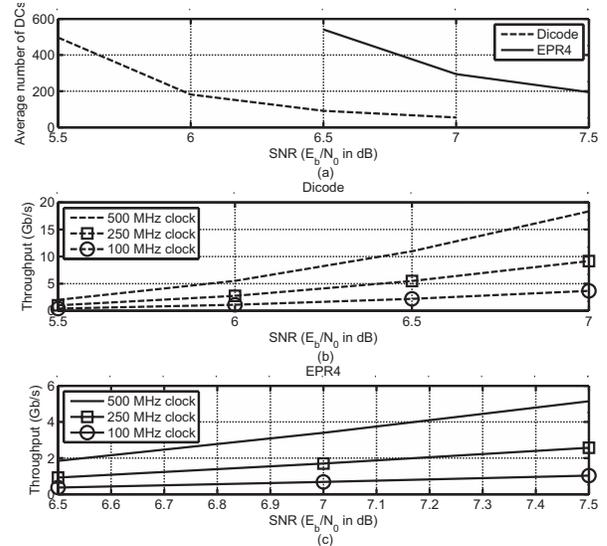


Figure 6. (a) Average number of decoding cycles used at different SNRs. (b) Estimated (core) throughput for joint decoding of the (2000,1000) LDPC code and the dicode channel, and (c) the (2000,1000) LDPC code and the EPR4 channel.