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CMRR REPORT

Center for Magnetic Recording Research

Contents

RESEARCH HIGHLIGHT

Quantized Iterative Message Passing Decoders with Low Error Floor for LDPC Codes

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University of California, San Diego

Introduction

Low-density parity-check (LDPC) codes have been the focus of much research over the past decade as a consequence of their near Shannon-limit performance under iterative message-passing (MP) decoding [1] . However, the error floor phenomenon has hindered the adoption of LDPC codes and iterative decoders in some applications requiring very low error rates. Roughly speaking, an error floor is an abrupt change in the slope of the error-rate performance curve of an MP decoder in the high SNR region. Since many important applications, such as data storage and high-speed digital communication, often require extremely low error rates, the study of error floors in LDPC codes remains of considerable practical, as well as theoretical, interest.

LDPC codes are usually represented by a Tanner graph, as shown in Figure 1. Variable nodes represent codeword bits and check nodes represent parity-check constraints. The degree of a node refers to the number of edges adjacent to it. An LDPC code has the property that the node degrees are small relative to the codeword length.

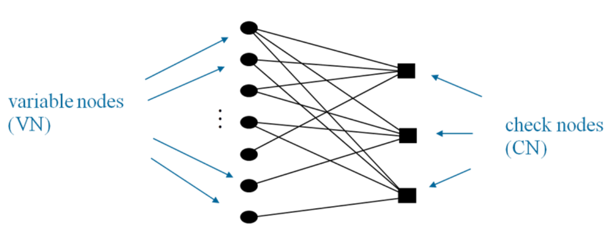


Figure 1. Tanner graph representation of LDPC codes

Optimal decoding of powerful LDPC codes is impractical, but suboptimal iterative message-passing (MP) decoding algorithms, such as the sum-product algorithm (SPA) and the min-sum algorithm (MSA), have been found to offer a useful tradeoff between decoder implementation complexity and error-rate performance.

From the Director

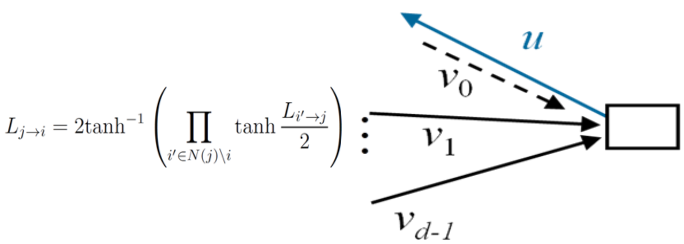
This newsletter comes at a time of many new and returning faces to CMRR. We welcome two new visiting scholars, Professor Stephane Mangin from Institut Jean Lamour at the University of Lorraine in France who will be spending a year at CMRR and Dr. Charles Sheppard of University of Johannesburg who will be visiting for three months. We also have five new graduate students starting their Ph.D. research this fall, as well as five new visiting students. We also have two new staff members, Patty Chang and Kelly Huang, who are helping fill the shoes of Kevin Wong, our fund manager for the last year who accepted a new position at general accounting. Welcome to all of you.

It was a bit more quiet than usual over the summer as we had 15 graduate students participating in summer internships with a range of companies- including eight students at Western Digital, two at Qualcomm, and one each at General Atomics, Microsoft Research, LSI Corporation, Ansys-HFSS, and MaNEP. Their summer research covered topics ranging from spintronic devices, hard drive tribology, advanced coding and signal processing, micromagnetic studies of hard drive technologies, metamaterials and application, to the characterization of flash memory. These topics reflect much of the current research at CMRR that will be presented in the upcoming 2012 Fall review. I'm particularly pleased to see the strong interaction of our students with our industrial partners as a clear part of the CMRR mission to train students for the information technology industries. Given the strong demand for our students, I would encourage companies interested in CMRR students for summer interns to contact me or other CMRR faculty sooner than later. I hope we can keep this strong participation of our students with our corporate sponsors growing in the coming years.

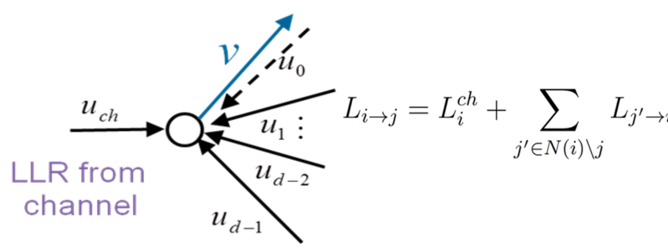
We continue to expand our educational efforts by organizing various conferences and workshops, as highlighted in the newsletter. Paul H. Siegel and Steve Swanson have organized the Non-Volatile Memories Workshop (NVMW) each of the last three years and the NVMW 2013 will be held from March 3-5. The workshop provides a unique showcase for outstanding research on solid state, non-volatile memories. Last spring, CMRR organized the International Workshop on Advanced Micromagnetics (IWAM) as a showcase for new and emerging techniques in the micromagnetic analysis of magnetic materials and devices. For next summer, we are organizing the International French-US Workshop- Toward Low Power Spintronic Devices– which is to be held from July 8-12. This workshop will include participation from academic institutions, Nobel Prize winner Albert Fert, leading industry representatives, start-up companies, funding agencies and venture capitalists. The participants will discuss new research developments and initiate new research conferences. We plan on having more of these workshops in future years as part of future research reviews and would like input on potential topics.

Eric E. Fullerton

The iterative decoder alternates between two phases, a "CN-to-VN" phase during which CNs send messages to their adjacent VNs, and a "VN-to-CN" phase during which VNs send messages to CNs along their adjacent edges. The message update rules, which we will now briefly describe for the SPA, are depicted schematically in Figures 2 and 3, respectively. In the figures, the set of neighboring CNs of VN i is denoted by $N(i)$, and the set of neighboring VNs of CN j is denoted by $N(j)$. In the initialization step of the decoding process, VN i forwards the same message to all of the CNs in $N(i)$, namely the log-likelihood ratio (LLR) L_i^{ch} derived from the corresponding channel output. In the CN-to-VN message update phase, CN j uses the incoming messages and the message update rule shown in Figure 2 to compute and forward, to VN i in $N(j)$, a new "CN-to-VN" message, $L_{j\to i}$. VN i then processes its incoming messages according to the update rule shown in Figure 3 and forwards to each adjacent CN an updated "VN-to-CN" message, $L_{i\to j}$. After a prespecified number of iterations, VN i sums all of the incoming LLR messages to produce an estimate of the corresponding code bit i. Note that all of the "CN-to-VN" message updates can be done in parallel, as can all of the "VN-to-CN" message updates. This enables efficient, high-speed software and hardware implementations of the decoding algorithm.



<u>Figure</u> 2. CN-to-VN message update: Each CN receives log-likelihood ratio (LLR) information from all of its neighboring VNs. For each such neighboring VN, it generates an updated "check-to-variable" message using the inputs from all other neighboring VNs.



<u>Figure</u> 3. VN-to-CN message update: Each VN receives log-likelihood ratio (LLR) information from all of its neighboring CNs. For each such neighboring CN, it generates an updated "variable-to-check" message using the inputs from all other neighboring CNs.

Trapping Sets and Error Floors

Error patterns in the error floor region often correspond to sets of variable nodes that lie in subgraphs of the Tanner graph with special combinatorial structure. For the binary symmetric channel (BSC) and the AWGN channel, these sets and their induced subgraphs have been referred to as near-codewords, trapping sets, or absorbing sets. The term "trapping set" is often used generically in reference to such error-prone substructures. For example, Figure 4 shows the error floor of the rate-1/2, length-2640 Margulis code on the AWGN channel. Most SPA decoding failures in the error floor region for this code correspond to the two trapping sets shown in Figure 5. (See [2], [3].)

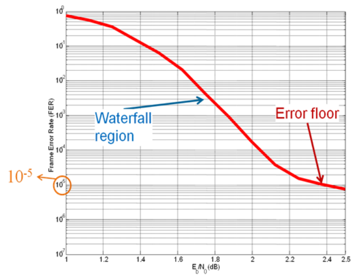
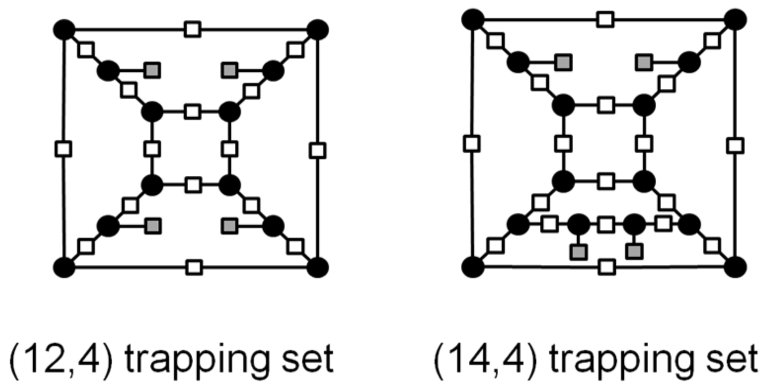


Figure 4. Error floor of Margulis code of length 2640, observed by Mackay-Postol in [2] and Richardson in [3] .

Figure 5. Two trapping sets correspond to the dominant errors in the error floor region for the rate-1/2, length-2640 Margulis code. The VNs in the trapping set are represented as solid black circles, and the CNs are represented as squares. If the variable nodes are set to the value 1, the CNs where parity-checks are not satisfied are shown as shaded squares.

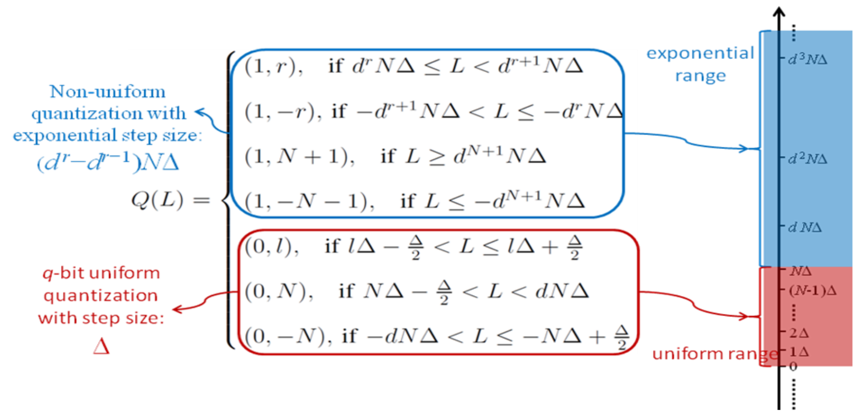


New Quantization Rule to Lower Error Floors

It is known that error floor characteristics also depend on system implementation issues, such as the quantization of channel LLR and message values, the decoding algorithm formulation, and the number of decoder iterations. In an idealized scenario, where all VNs outside the trapping set are assumed to have been correctly decoded, and where the VNs in the trapping set satisfy a certain separation assumption, we proved that decoders using the SPA and MSA could correct trapping set errors if the maximum magnitude of messages passed between nodes is not restricted [4] [5] .

However, in practice, the messages must be represented by a limited number of bits. Typically, decoder implementations use uniform quantization, which permits fine resolution over a limited range (i.e., large values are "clipped") or coarse resolution over larger range (i.e., message values are represented less accurately).

If, as our idealized analysis suggests, a large range of values needs to be represented, the precision of small messages would have to be sacrificed, significantly degrading the error-rate performance. To resolve this dilemma, we propose a new quantization method which allows fine resolution for small messages and somewhat coarser representation over a range of larger messages. This method, which we call (q+1)-bit quasi-uniform quantization, is portrayed graphically in Figure 6. The corresponding quantization table for q=3 is shown in Figure 7. We assume here that the Tanner graph is VN-degree regular, meaning that all variable nodes have the same degree, d_v; however, similar analytical results and quasi-uniform quantization techniques can be applied to LDPC codes with different VN-node degrees.



<u>Figure</u> 6. (q+1)-bit quasi-uniform quantization, where $N = 2^{q-1}-1$, $-N+1 \le l \le N-1$, $1 \le r \le N$, Δ is the nominal step size, and d is a quantization parameter within the range $(1, d_v - 1]$.

3-bit uniform quantization with step size: 1

3-bit exponential quantization step size: $3\cdot(3^r - 3^{r-1})$

Messages	Ranges	Values
(0,000)	(-0.5, 0.5]	0
(0,001)	(0.5, 1.5]	1
(0,010)	(1.5, 2.5]	2
(0,011)	(2.5, 9)	3
(1,000)	[9, 27)	9
(1,001)	[27, 81)	27
(1,010)	[81, 243)	81
(1,011)	[243, ∞)	243

Max magnitude in 4-bit uniform quantization with step size 1 is only 7

<u>Figure</u> 7. An example of (3+1)-bit quasi-uniform quantization, where Δ = 1, d = 3, for the positive range of message values.

Numerical Results

Figure 8 shows SPA performance results for a rate-0.3, length-640, quasi-cyclic LDPC code on the AWGN channel, with a maximum of 200 decoder iterations. We can see that the proposed quantization performs even better than floating-point SPA due to its faster convergence. Note that the slope of the error rate curve of the (5+1)-bit quantized SPA is the same as the LP decoder, which is steeper than the floating-point SPA curve.

In Figure 9, we show results for the rate-0.5, length-2640 Margulis code. In this decoder performance comparison, we also considered the "dual quantization" SPA decoding technique proposed in [6] . In dual quantization, two uniform quantization rules with different step sizes are used in CN-to-VN message update. Specifically, using the notation of [6], Q*m*.*f* quantization uses a signed fixed-point number with *m* bits to the left of the radix point to represent integer values, and *f* bits to the right of the radix point to represent fractional values. For example, a Q4.2 quantizer has uniform quantization step size of 0.25 and a range of [-7.75, 7.75].

In the figure, we see that the proposed (5+1)-bit quasi-uniform quantizer has the best error-floor performance; it even improves upon the 64-bit double-precision floating-point SPA decoder in the low error-rate region as a result of its faster convergence.

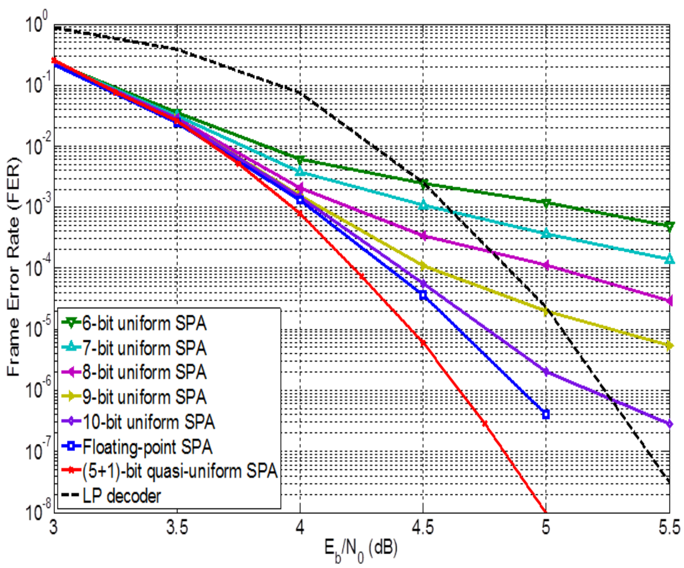


Figure 8. FER results of SPA decoder on the (640,192) QC-LDPC code on AWGNC. The uniform quantization step Δ = 0.25 and the exponential step parameter *d* = 1.5 in the (5+1)-bit quasi-uniform quantization. The maximum number of iterations is 200.

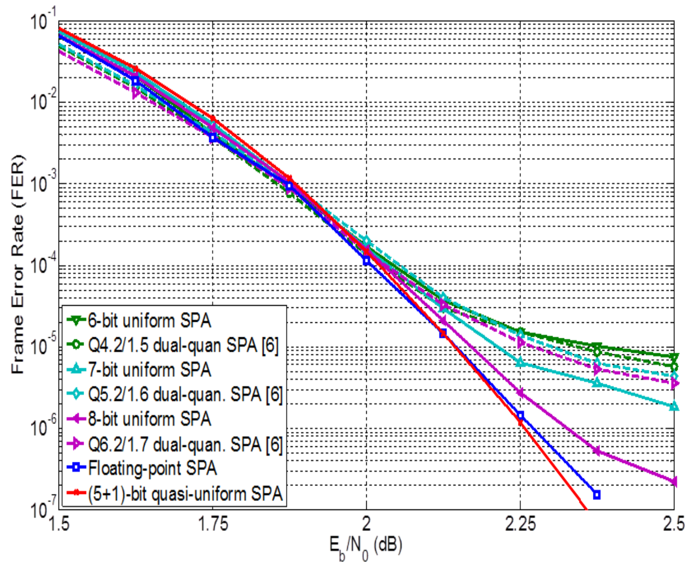


Figure 9. FER results of approximate-SPA decoder on the Margulis code of length 2640 on AWGNC. Uniform quantization step Δ = 0.25 and the exponential step parameter *d* = 1.3 in the (5+1)-bit quasi-uniform quantization. The maximum number of iterations is 200.

Summary and Conclusions

In this research, we have shown that the use of uniform quantization in iterative message-passing decoding can be a significant factor in the appearance of error floors in LDPC code performance. To address this problem, we have proposed a new quasi-uniform quantization method that effectively extends the dynamic range of the quantized message values. Without modifying the CN-to-VN and VN-to-CN message update rules or adding extra stages to standard iterative decoding algorithms, the use of quasi-uniform quantization was shown to significantly lower the error floors of two well-studied LDPC codes.

References

[1] R. G. Gallager, “Low-density parity-check codes,” *IRE Trans. Inform. Theory*, vol. 8, pp. 21-28, Jan. 1962.

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[3] T. Richardson, “Error-floors of LDPC codes,” in *Proc. 41st Annual Allerton Conference on Communication, Control, and Computing*, Monticello, IL, Oct. 1-3, 2003, pp. 1426-1435.

[4] X. Zhang and P. Siegel, "Quantized min-sum decoders with low error floor for LDPC codes," in *Proc. IEEE Int. Symp. Inform. Theory* (ISIT), Cambridge, MA, July 2-5, 2012, pp. 2871-2875.

[5] X. Zhang and Paul Siegel, "Will the real error floor please stand up?" in *Proc. IEEE Int. Conf. Signal Processing and Commun.* (*SPCOM*), Bangalore, India, July 22-25, 2012.

[6] Z. Zhang, “Design of LDPC decoders for improved low error rate performance,” Ph.D. dissertation, University of California, Berkeley, 2009.

NVMW 2013

Call for Presentations

4th Non-Volatile Memories Workshop

La Jolla, California USA

March 3-5, 2013

http://nvmw.ucsd.edu

Organizers
Steven Swanson, UCSD CSE
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The 4th *Annual Non-Volatile Memories Workshop* (NVMW 2013) provides a unique showcase for outstanding research on solid state, non-volatile memories. It features a "vertically integrated" program that includes presentations on devices, data encoding, systems architecture, and applications related to these exciting new data storage technologies. Last year's workshop (NVMW 2012) included 32 speakers from top universities, industrial research labs, and device manufacturers and attracted nearly 200 attendees. (The website for NVMW 2012 can be found at http://nvmw.ucsd.edu/2012.) NVMW 2013 will build on this success.

The organizing committee is soliciting presentations on any topic related to non-volatile, solid state memories, including:

- Advances in memory devices or memory cell design.
- Characterization of commercial or experimental memory devices.
- Error correction and data encoding schemes for non-volatile memories.
- Advances in non-volatile memory-based storage system.
- New applications of non-volatile memories.
- Operating system and file system designs for non-volatile memories.
- Non-volatile storage system performance measurements.
- Security and reliability of solid-state storage systems.

The goal is to facilitate the exchange of the latest ideas, insights, and knowledge that can propel future progress. To that end, presentations may include new results or work that has already been published during the 18 months prior to the submission deadline. In lieu of printed proceedings, we will post the slides and extended abstracts of the presentations online. Presentation of new work at the workshop does not preclude future publication.

Workshop submissions should be in the form of a 2-page presentation abstract. Submissions will be evaluated on the basis of impact, novelty, and general interest. **The submission deadline is November 12, 2012, with notification of acceptance by January 31, 2013.**

Further details on abstract submission, technical program, tutorials, travel, social program, and travel grants will be provided at the workshop website:

http://nvmw.ucsd.edu

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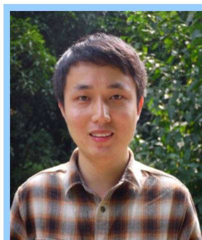
Visiting Scholars

Professor **Stephane Mangin** is a visiting scholar in Prof. Eric E. Fullerton's group from the Institut Jean Lamour at University of Lorraine. His research project "Optical Probe and Manipulation of Magnetization at the Nanometer Scale" will focus on fundamental scientific issues of spin manipulation in nano-structured magnetic materials subject to optical/magnetic excitations and further provide the scientific underpinnings for the next generation of heat-assisted magnetic recording (HAMR).

Dr. Charles Sheppard received his doctorate in Physics from the University of Johannesburg in 2008, with his thesis: "Formation of CuIn(Se, S)2 and Cu(In, Ga)(Se, S)2 thin films by Chalcogenization of Sputtered Metallic Alloys." He joined the Cr group at the end of 2008. The Cr research group's current research activities focus on quantum criticality and the possible coexistence of super conductivity and antiferromagnetism within Cr and its alloys.

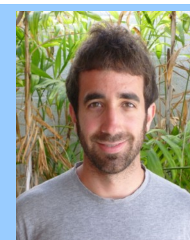
Visiting Graduate Students



Lei Yang is currently a graduate student at Xi'an Jiaotong University in China, majoring in Mechanical Engineering. In the fall of 2009, he joined the research group of Prof. Dongfeng Diao in Xi'an. Now he is a visiting graduate student advised by Prof. Talke. His research will focus on the mechanism of data loss and the demagnetization of high density magnetic recording disk under sliding contact.

Masoud Alipour is a graduate student at EPFL, Switzerland, where he is completing his Ph.D. under the supervision of Amin Shokrollahi. He worked on Linear Programming Decoding in Paul H. Siegel's group. He received his B.S. in Applied Mathematics from Shahid Beheshti University, Tehran, Iran in 2003. He moved to Switzerland where he obtained his Master's degree in computer science in 2007. His research interests include iterative decoding, rateless codes and their applications.

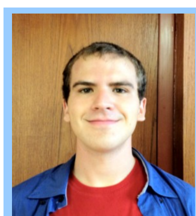
Peng Zuo is currently a Ph.D. student at Tsinghua University in China, majoring in Electrical Engineering. He is a visiting student advised by Professor Vitaliy Lomakin. His research area is Computational Electromagnetics. He is currently doing research on how to improve the accuracy and stability of the Electromagnetic Finite Element Method in the Transient Eddy Current Field.



Jon Ander Arregi is currently a graduate student at the Nanomagnetism group at CIC nanoGUNE in Donostia, where he studies the nanoscale magnetic phenomena by means of magneto-optical effects. He joined the Fullerton Lab for the fall 2012; his research will focus on thin-film and nanostructure fabrication as well as characterization of FeRh, a promising material for its implementation in heat assisted magnetic recording devices.

Chuanwei Zhang is a Ph.D. student at Harbin Institute of Technology in China, majoring in Mechanical Design. He received his B.A. at Xi'an Jiaotong University in 2007, then he joined the laboratory of Aerospace Tribology in Harbin. Now he is a visiting graduate student advised by Professor Frank E. Talke. His research will focus on studying the wear characteristics and tribology of the head disk interface, including the dimple gimbal interface.

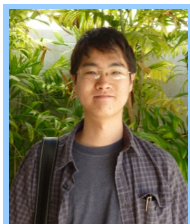
New Graduate Students



Robert Tolley is a 1st year Ph.D. student in Electrical and Computer Engineering, and is a part of the Fullerton research group. He received his M.S. in Physics from Miami University in 2012, working in the Eid group on experimental transport properties of thin-film ferromagnetic semiconductors and transport in nonmagnetic nanostructures. His research interests include development and characterization of thin film magnets and magnetic structures.

Welcome!

Young Jin Kim is a 1st year graduate student in the Materials Science and Engineering Ph.D program at UCSD. He received his B.S degree in Mechanical Engineering from UCSD. As an undergraduate student, he worked in Prof. Joanna McKittrick's Lab and with Prof. Sungho Jin's Group. Now he joins Prof. Sungho Jin's group as a Ph.D student and his research interest is in the synthesizing of nano size magnetic power using spark erosion technique.



Young Woo Seo received his Bachelor's degree in Mechanical Engineering from the University of California, San Diego in 2012. He is currently a graduate student in the Mechanical and Aerospace Engineering department, where he is studying to get a Master's degree in Mechanical Engineering. He joined the Talke Lab in the summer 2012. His first experiment involves the study of dimple/gimbal interface in a hard disk drive.

Visiting Undergraduate Student

Hannes Dikel is an undergraduate student at the Technical University Munich (TUM) in Germany, majoring in Medical Engineering. In the summer of 2012, he joined Prof Talke's group as a visiting student. Currently he is working on developing a new measurement technique for measuring the dimensions of the ossicles for stapes

New Staff Members

Patty Chang is currently a Psychology student here at UCSD. She is planning on going into nursing after she graduates Fall 2012. In her free time, she enjoys baking and traveling.

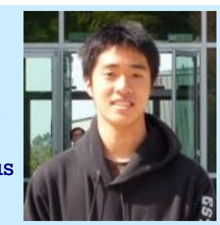
Kelly Huang is a second year undergraduate student at University of California, San Diego. She is currently majoring in Human Development and thinking about double majoring in Cognitive Science.

Cihan Kuru received his B.S. in Physics from Balikesir University in 2007.He is currently a graduate student in Materials Science and Engineering.He joined Prof. Jin's group in 2010 where he studied electronic and spintronic properties of graphene.He explores the implementation of graphene to the spintronic devices as well as field effect transistors.

Bing Fan received her B.S. degree in Electrical and Computer Engineering from Shanghai Jiao Tong University, Shanghai, China, in 2011. She is currently working in Prof. Siegel's STAR group, as a Ph.D. student. Bing is interested in coding theory. Her research focuses on TDMR and LDPC codes. She enjoys travelling and swimming.

New Undergraduate Students

Nigel White is a fourth year undergraduate student here at University of California, San Diego. He is currently majoring in physics. Nigel is originally from Orange County, California. His interest involves working with condensed matter and superconducting systems.



Matthew Hu is a third year undergraduate studying Electrical Engineering at the University of California, San Diego. He plans to obtain his B.S. by 2014 and pursue his M.S. immediately afterwards. His current focus is on working with Cubit, the FastMag preprocessor, and writing code for other simulation software.

Karcher Morris is an undergraduate senior at UCSD pursuing degrees in both Aerospace Engineering and Management Science. This previous spring and summer he has worked wihin Professor Talke's Tribology Lab focusing on fretting wear experiments and analysis at the dimple/gimbal surface in the hard disk drive as well as a "Deep Contact" model for flying height simulation.


International French-US Workshop
Toward Low Power Spintronic Devices
July 8th – 12th, 2013 in La Jolla, California
The aim of this workshop is to gather the scientific and engineering communities on the fast growing field of spintronic and its applications. The workshop will cover the innovation process from scientific knowledge to new products such as STT-MRAM; oscillators and novel magnetic memory and logic structures. It will provide attendees opportunities to discuss new developments and to initiate collaborations and research projects. The workshop will benefit from the attendance of well-known contributors from academic institutions, leading industries , start-up companies and also from funding agencies and venture capital firms.
A special session will be dedicated to fostering research cooperation between France and US researchers with emphasis on 3 domains: fundamental science, innovation and education of the next generation of scientists
Invited speakers
A. FERT (Nobel Prize 2007): CNRS/ Thales (France) *
H. OHNO: Tohoku University (Japan)
J. Z. Sun: IBM-Yorktown Height (USA)
J.ÅKERMAN: University of Gothenburg(Sweden)
K. LEE: Qualcom- San Diego (USA)*
A.HOFFMANN: Argonne National Laboratory (USA)*
Y. OTANI: University of Tokyo and RIKEN (Japan) *
L.VILA: INAC-CEA (France)
D.L STEIN: New York University (USA)
S.S.P. PARKIN : Stanford / IBM –Almaden (USA)
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Y. SUZUKI: Ozaka University (Japan)
L. PREJBEANU : Crocus (France)
D. APALKOV: Grandis (USA)
V. LOMAKIN: UC San Diego (USA)*
*confirmed speakers
30 minute presentations for invited speakers, 15 minute presentations for selected contributing speakers, and a poster session will allow subjects to be discussed in depth.
Abstracts (see template online) must be submitted before March 1, 2013. Posters and oral presentations will be selected by the scientific committee and authors will be informed of the selection by April 1st.
Registration will be accepted until June 1st
http://nanomag.ucsd.edu/iwst/
Scientific committee
•E. E. Fullerton : University of California, San Diego
•A. Kent : New York University
•S. Mangin : Université de Lorraine, Nancy
•J.P. Nozière : Spintec
•D. Ravelosona : Institut d'Electronique Fondamentale
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Organizing committee
I. Villanueva : University of California San Diego
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Selected Papers and Talks

Research Professor Ami E. Berkowitz

P. K. Nguyen, K. H. Lee, S. I. Kim, K. A. Ahn, L. H. Chen, S. M. Lee, R. K. Chen, **S. Jin**, **A. E. Berkowitz**, "Spark erosion: a high production rate method for producing $Bi_{0.5} Sb_{1.5}Te_3$ nanoparticles with enhanced thermoelectric performance" *Nanotechnology* Vol. 23, 415604, 2012

Professor Raymond A. de Callafon

U. Boettcher, D. Fetzer, H. Li, **R. A. de Callafon**, **F. E. Talke**, "Reference signal shaping for closed-loop systems with application to seeking in hard disk drives" *IEEE Transactions on Control Systems Technology* Vol. 2, 335-45, March 2012

U. Boettcher, L. Matthes, B. Knigge, **R.A. de Callafon**, **F.E. Talke**, "Suppression of cross-track vibrations using a self-sensing micro-actuator in hard disk drives" *Microsystem Technologies* Vol. 18 No. 9-10, 1309-17, September 2012

L. Matthes, U. Boettcher, B. Knigge, **R. A. de Callafon**, **F. E. Talke**, "Contact and temperature rise of thermal flying height control slider in hard disk drives" *Microsystem Technologies* Vol. 18 No. 9-10, 1693-701, September 2012

Professor Eric Fullerton

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Not shown: Jon Anders Arregi, Sohini Manna, Youyi Fu, Isaac Liu, Minghai Qin

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Student	Level	Advisor	Dept.	Area of Research
Xiaojie Zhang	Ph.D.	Prof. Paul H. Siegel	ECE	Structural analysis and decoding techniques for LDPC codes
Adrian Caulfield	Ph.D.	Asst. Prof. Steve Swanson	CSE	Architecting optimized I/O systems by designing across the hardware/software boundary, with a focus on efficiently integrating high performance, low latency non-volatile memories into computer systems.
Laura M. Grupp	Ph.D.	Asst. Prof. Steve Swanson	CSE	Optimizing the management layer inside flash-based SSDs through detailed characterization of flash chips.

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