University of California, San Diego ISSN: 0888-7381

CMRR Report

Center for Magnetic Recording Research

Number 31 Winter 2009

Research Highlight

Error Correction Coding for Flash Memories

Contents:

Young Engineer of the Year

Left to Right: Gary Jin and Kaizhong Gao

Dr. Kai-Zhong Gao, a CMRR graduate, was recently named the 2009 Minnesota Young Engineer of the Year by the Minnesota Federation of Engineering, Science and Technology Societies.

Kai-Zhong is currently a Senior Engineer Manager at the Seagate R&D facility in Bloomington, Minnesota, where he and his group explore advanced magnetic recording technologies. Kai-Zhong came to CMRR in 1997 as a member of Professor Neal Bertram's Magnetic Recording Physics and Micromagnetics Group. He received his Ph.D. in November 2002. His thesis, "Optimization of Write Heads and Media for Ultra High Density and Data Rate Magnetic Recording," focused on perpendicular recording systems.

This is not the first prestigious honor that Kai-Zhong has received. In 2003, Kai-Zhong was awarded the CMRR Sheldon Schultz Prize for Excellence in Graduate Student Research for distinguishing himself through the creativity of his research and the impact of his publications. He was also co-recipient with Professor Bertram of the 2004 Information Storage Industry Consortium (INSIC) Technical Achievement Award.

All of Kai-Zhong's colleagues at CMRR are proud of his accomplishments. He is an excellent example of the caliber of students who graduate from CMRR each year.

Please join us in congratulating Kai-Zhong.

Left to Right: Professors Jack Wolf & Robert Gray, and Professor Emeritus Andrew Viterbi

2009 Shannon Memorial Lecture

Robert M. Gray, the Alcatel/Lucent Technologies Professor of Communications and Networking in the School of Engineering and Professor of Electrical Engineering, at Stanford University, presented the 7th Annual Shannon Memorial Lecture on April 21, 2009.

His lecture, entitled "Shannon Source Coding, Ornstein Isomorphism, and Random Process Models," addressed the impact of Shannon's ideas of entropy and coding on ergodic theory, the theory of measure preserving (and related) transformations on probability spaces.

Lecture available at: http://video-jsoe.ucsd.edu/asx/ShannonMemorialLecture2009RobertGray.asx

Shannon Memorial Fellowship Awarded

Yuzhe Jin, a Ph.D. student of ECE Professor Bhaskar Rao, is the recipient of the 2009-2010 Shannon Memorial Fellowship. The purpose of this endowed fellowship is to honor an outstanding graduate student at UCSD whose research is in the field of information theory.

Mr. Jin came to UCSD in the fall of 2005 from Tsinghua University where he obtained a Bachelors degree.

His current work involves the interface between network information theory and sparse signal recovery problems that arise in compressed sensing and other applications.

Left to Right: CMRR Professor Jack Wolf and Yuzhe Jin

Talke Inducted into Acatech

Frank E. Talke, an Endowed Chaired Professor at CMRR has been inducted into the Academy der Technikwissenschaften (Acatech). The Academy is the equivalent of the National Academy of Engineering in the United States. Members are nominated and voted on by all 296 members of the Acatech.

The Acatech brings together the best minds in science and business. The members are admitted into the organization based on their outstanding scientific achievements and excellent reputation. Since Acatech handles a broad spectrum of interdisciplinary issues in science and technology, members stem from the engineering and natural sciences, the humanities and the social sciences.

Professor Talke was officially inducted into Acatech in March 2009.

From the Director

A lingering recession, a spreading flu virus, and global unrest - these are certainly trying times. At CMRR, though, we are working hard, and successfully, to advance the frontiers of information storage technology and systems. Motivated by the never-ending need for storage systems with greater capacity, performance, and security, our research agenda continues to cover a broad spectrum, ranging from fundamental studies of magnetic materials to device-level data security.

With the decline in the number of players in the disk and tape storage industry - witness the recent sale by Fujitsu of its disk drive business to Toshiba - we have redoubled efforts to strengthen existing industrial partnerships while actively seeking and pursuing new opportunities. Several CMRR investigators, as well as teams of CMRR-affiliated faculty, have been active in submitting research proposals to the National Science Foundation (NSF), the National Security Agency (NSA), the UC Discovery Grant Program, and the recently established UC-Labs Research Program. Several of these have already been approved. The projects run the gamut from computational and experimental investigations of magnetic nanostructures; to integrated head, media, channel, and servo design for bit-patterned media recording; and to signal processing and coding methods for multidimensional recording technologies. We are also planning a concerted effort to capture our share of the research funding infused by the federal stimulus package.

Many of these projects expand and diversify our research portfolio, reflecting our responsiveness to new trends in data storage technology. For example, in the area of flash memory, we have initiated a collaboration with Prof. Steve Swanson, a member of the Computer Science and Engineering Department, and several other non-UCSD colleagues. We have extended the scope of our Secure Erasure project to include flash-based devices and, using experimentally measured error data, we are exploring new error-correction and energy-efficient coding techniques for future generations of flash memories. (See the Research Highlight in this issue.) We have also partnered on a proposal that addresses novel flash-based storage system architectures for data-intensive computing.

The relevance and impact of our technical efforts at CMRR continue to receive both internal and external recognition, evidence of which you will find throughout this newsletter. Most notable is the selection of one of our graduates, Dr. Kai-Zhong Gao of Seagate Technology, as the 2009 Minnesota Young Engineer of the Year, and the induction of Prof. Frank Talke into Acatech, the German equivalent of our National Academy of Engineering.

Looking beyond our research activities, the Spring season also reminds us of CMRR's many contributions to the UCSD campus and the larger San Diego community. April featured the presentation of the 7th Annual Shannon Memorial Lecture and the awarding of the 2nd Annual Shannon Memorial Fellowship. Both of these traditions originated from CMRR, and continue to be sponsored by CMRR in cooperation with Calit2 and the Information Theory and Applications (ITA) Center at UCSD. And, earlier in the month, Associate Director Nate Heintzman, along with a team of CMRR graduate students and researchers, organized and hosted a very well-attended exhibit - "The Incredible Shrinking Hard Drive" - at the inaugural San Diego Science Festival in Balboa Park.

To conclude, let me remind you that partnerships with the private and public sectors provide the foundation for the technical innovation, creation of human capital, and societal contributions that are the hallmarks of CMRR. Inquiries about possible collaborations are always welcome.

Now, please enjoy this issue of CMRR Report.

Paul H. Siegel

Research Highlight ERROR CORRECTION CODING FOR FLASH MEMORIES

By Eitan Yaakobi, Jing Ma, Adrian Caulfield, Laura Grupp, Steven Swanson, Paul H. Siegel, and Jack K. Wolf, *University of California, San Diego*

Introduction

Data storage devices rely upon error detection and correction (EDAC) codes to ensure highly reliable information retrieval. Optical storage devices, such as CD- and DVD-based recorders, allocate significant overhead for the redundancy introduced by the encoding of data into codewords. High-performance hard disk drives also devote substantial overhead for EDAC codes that can correct multiple erroneous bytes within a codeword. The powerful codes used in these storage devices are the culmination of decades of research and development, and efforts to design more powerful and efficient EDAC coding algorithms are ongoing.

Non-volatile, solid-state NAND-flash memory devices are finding use in an increasing number of computing and consumer electronic devices. They have replaced hard drives in many of these applications because of their high data-transfer rates, mechanical durability, and low power consumption. They are also being combined with disk drives in so-called "hybrid drives" that take advantage of the benefits offered by both types of non-volatile storage media.

Flash memory chips may use single-level cell (SLC) technology, where each cell can store one binary digit, or multi-level cell (MLC) technology, where each cell can store multiple binary digits. To date, flash storage devices have used only low-redundancy EDAC codes that offer minimal error correction and detection capabilities, such as single bit-error correcting Hamming codes and error-detecting cyclic redundancy check (CRC) codes. The demand for increased storage capacity, coupled with the introduction of MLC flash technology, has created the need for more powerful coding methods using, for example, Bose-Chaudhuri-Hocquenghem (BCH) codes and Reed-Solomon (RS) codes.

To help address this need, we used an extensive empirical database of errors observed during write, read, and erase operations on a flash memory device to develop a more comprehensive understanding of the error mechanisms and error characteristics of this increasingly important storage technology.

Flash Memory Structure

A flash memory chip is built from *floating-gate cells* which are organized in *blocks*. Each block contains either 64 *pages* (SLC) or 128 pages (MLC), where the size of a page is 2KB [3]. A chip holds an array of thousands of blocks. One of the distinctive properties of flash memory is its read-write asymmetry: it is easy to read an individual page, but overwriting a previously written page requires the erasure of the entire block containing the page, followed by the rewriting of the entire contents of the block, including the updated page [3]. This erase-rewrite operation incurs a substantial cost in time and power consumption. Moreover, repeated block erasures degrade flash memory performance, thereby limiting the useful lifetime of the device. In order to reduce the number of block erasure operations, an updated version of a stored page is simply written into another available physical location, and its previous location is marked as invalid. A table – called the *Flash Transition Layer* (*FTL*) [1, 5] – keeps a record of the latest mapping between logical and physical pages and is maintained in the memory device. When the memory becomes full, blocks no longer in active use need to be erased to allow new data to be stored [1]. To enhance device lifetime, "wear-leveling" algorithms are used to balance the number of erasures among blocks within a single device [3, 5].

Typically, each page in a flash memory block contains, in addition to its 2KB of data, a spare area of 64B. A portion of this spare area is used to store metadata in order to build the FTL once the flash memory is

activated [1]. The rest of the spare area can be used for storing the redundancy bytes of EDAC codes [4].

Description of Experiments

Error statistics were gathered from several blocks on SLC and MLC flash memory chips. For each block, we repeated the following process hundreds of thousands to millions of times:

1. Erase the block.
2. Write pseudorandom data into the block.
3. Read the block and identify errors by comparing the originally recorded data to the data that was read.

We first used the database of errors to compute the raw Bit Error Rate (BER) and raw Page Error Rate (PER) associated with each iteration of the measurement process. The results for both SLC and MLC devices are shown in Figure 1.

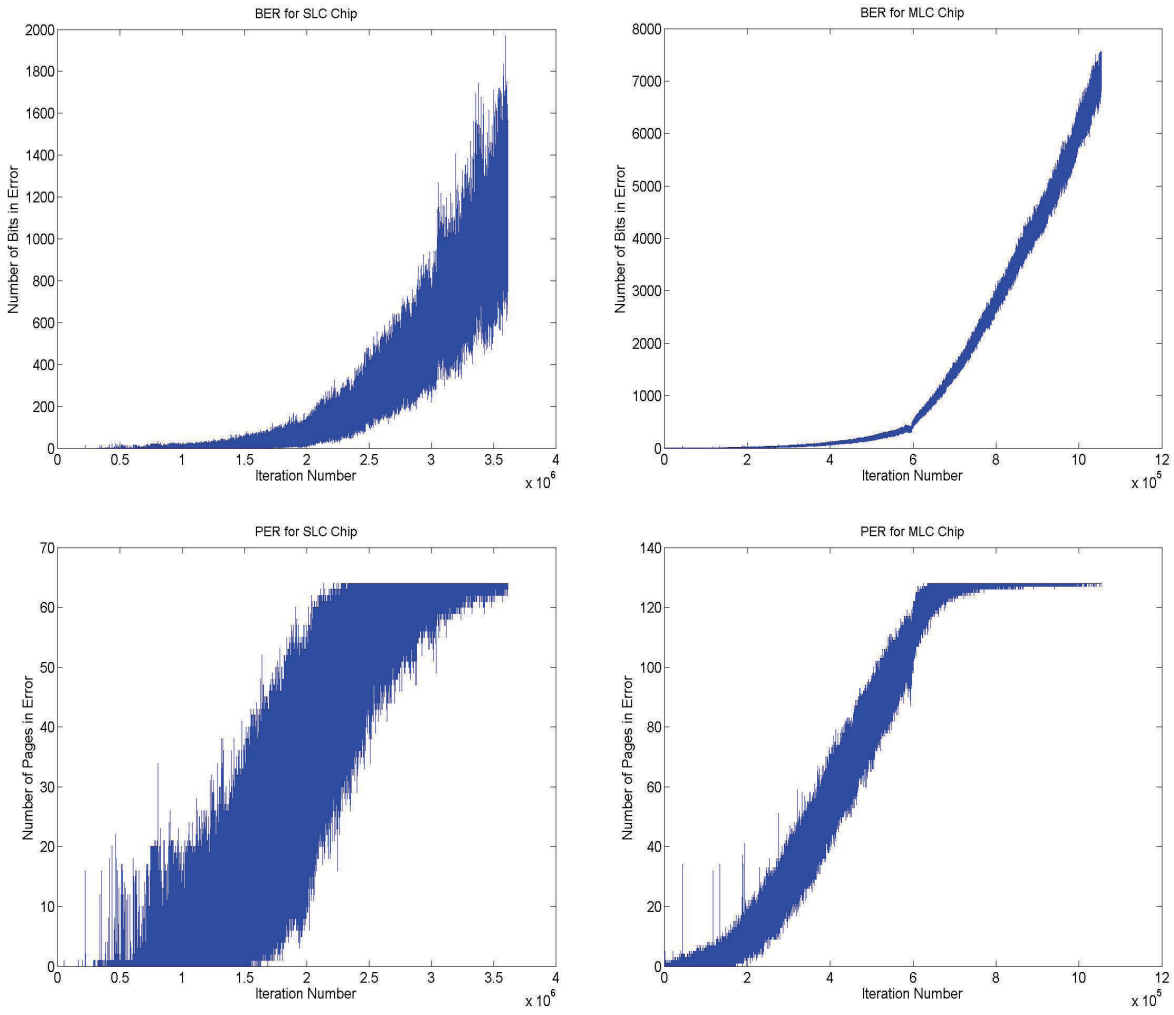


Figure 1. BER and PER for SLC and MLC chips

We then examined the data to determine if there was any asymmetry in the error process by comparing the number of times a written 0 was read as a 1 to the number of times a written 1 was read as a 0. We also studied the burstiness and data dependence of the observed errors. Finally, we used the error measurements to compare the performance of various error correcting coding (ECC) methods at the page level. Among the codes we considered were BCH and RS random-error correcting codes, as well as and burst-error correcting codes.

We now present preliminary results and conclusions from these investigations.

Error Asymmetry and Burstiness

The asymmetry between programming and erasing a flash cell suggests that there might be a corresponding asymmetry in the direction of errors [2]. A "plus" error is one where a bit of value 0 is read as a 1, and a "minus" error is one where a bit of value 1 is read as a 0. For each iteration, we compared the number of plus and minus errors in order to determine if one or the other of these error types was more prevalent. The results are shown in Figure 2 for both SLC and MLC chips. In both plots, the horizontal axis represents the iteration number and the vertical axis gives the difference between the number of plus and minus errors. For both SLC and MLC chips, we can see that the two types of errors are in essentially equal proportion.

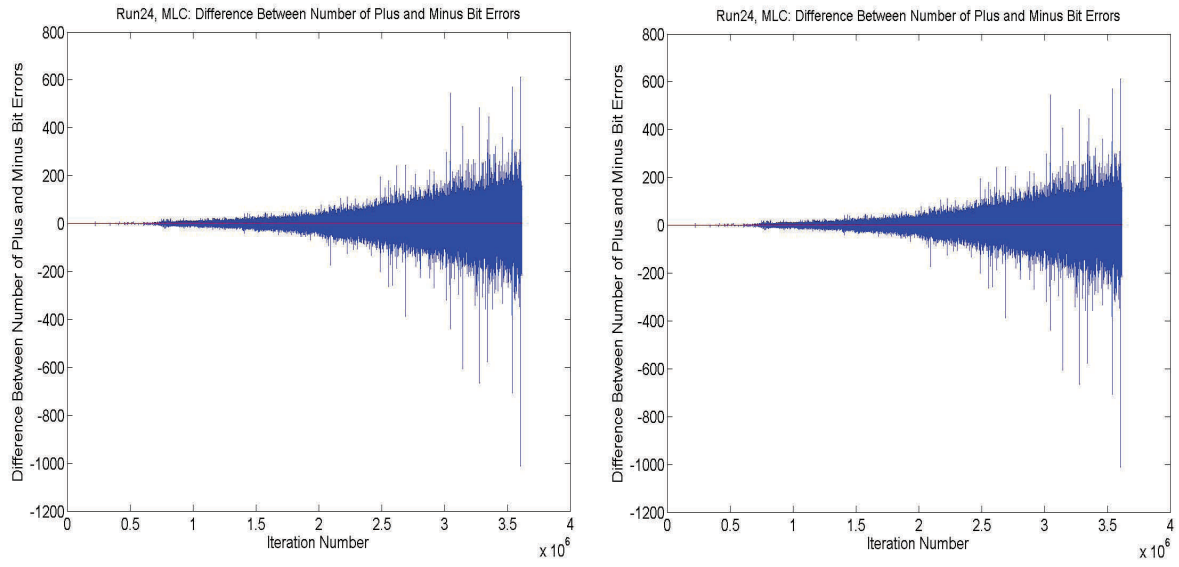


Figure 2. The difference between the number of plus and minus errors for SLC and MLC.

Another important characteristic of errors within a page is their degree of burstiness. One measure of burstiness is obtained by partitioning the page into non-overlapping "symbols" of a given length and counting the average number of bit errors per symbol. The results of such an analysis could help to determine, for example, the relative advantage or disadvantage of using a symbol-based RS code as compared to a bit-based BCH code.

A more easily computed indicator of possible burstiness of errors within a page is obtained by dividing the number of bit errors by the number of symbols. We computed this statistic as a function of the iteration number. In view of the length of a flash memory page, we subdivided each page into 11-bit symbols, thereby allowing the use of only one RS codeword per page. The results are shown in Figure 3, and they indicate that only a small percentage of the symbols that were in error contained more than a single bit error. This suggests that a bit-based BCH code might be more efficient in correcting errors within a page than a symbol-based RS code.

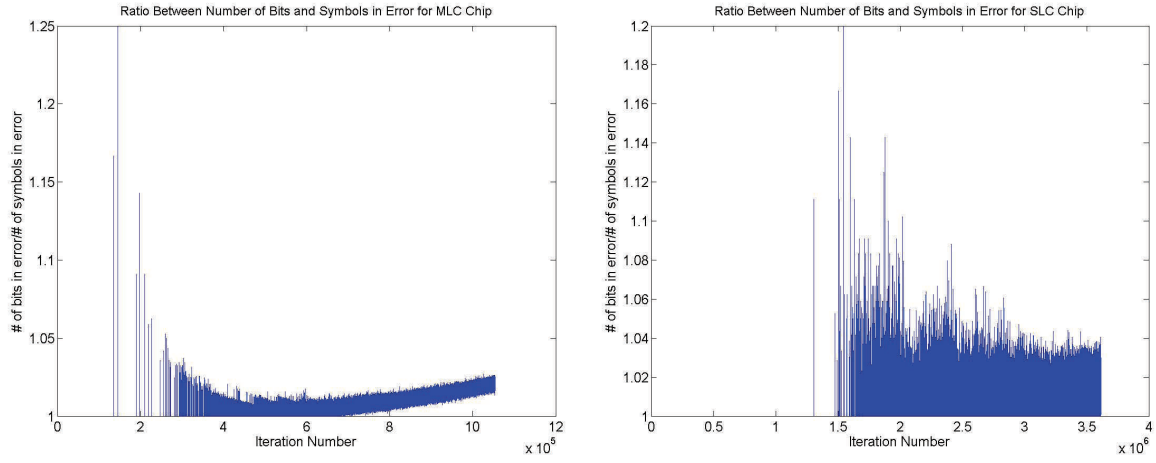


Figure 3. The ratio of number of bits in error and number of symbols in error

We also investigated the extent to which errors might be data dependent, that is, whether errors are more likely to appear within specific data patterns. Based on our previous results, we operated under the assumption that errors are likely to be locally isolated, meaning that none of the neighboring bits within a window surrounding the erroneous bit are in error. For each iteration, we examined the data written in a 7-bit window surrounding each error and counted the number of times each of the 128 possible 7-bit data patterns appeared in that window. The results for both SLC and MLC chips are plotted in Figure 4 as the occurrence percentage of each 7-bit pattern, given that the middle bit is in error. It appears that there is no strong dependence on the written data pattern, with occurrence percentages falling in the range of 0.765% to 0.796%.

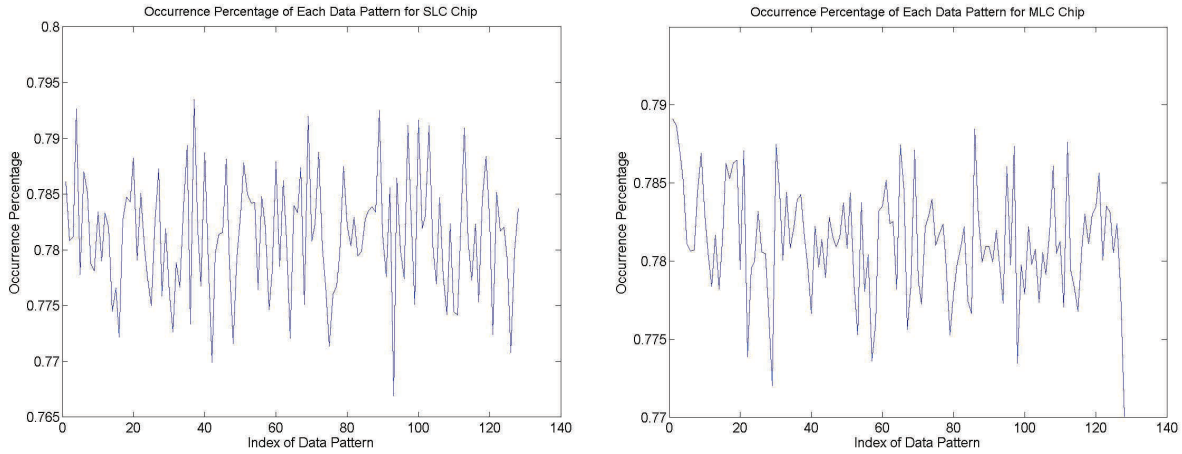


Figure 4. Occurrence percentage of 7-bit data patterns with middle bit in error for SLC and MLC chips.

ECC Comparison

We conclude from the preceding data analysis that bit errors in both SLC and MLC devices are likely to occur uniformly within a page, with no preferred symmetry or local data dependence. This suggests that to achieve the best performance within a block, a BCH code should be superior to a RS code or burst-correcting code. In order to test this conjecture, we can use the error database to compare the performance of representatives of these families of codes. As a first step in this direction, we determined, for each candidate code, the number of pages that experienced a larger number of errors than the code could correct. This provided an estimate of the page error rate (PER) for each code. Figure 5 shows the results for SLC and MLC chips, with a comparison of BCH codes to both RS codes and a burst-error correcting code. The plots suggest that for a fixed redundancy the best performance is achieved by using a BCH code.

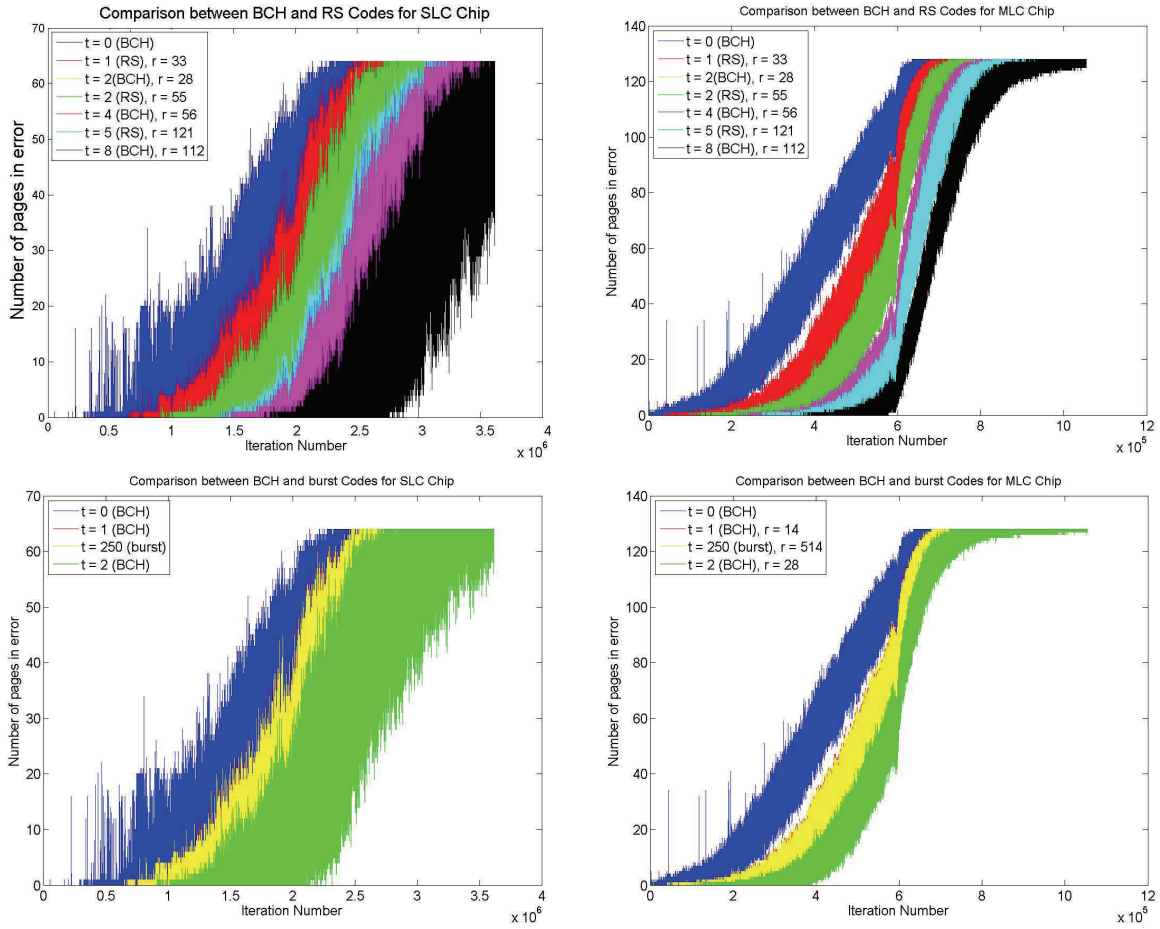


Figure 5. Comparison of the PER for BCH, RS, and burst correcting code

Summary and Conclusions

In this work, we used empirical data to investigate the characteristics of errors in SLC and MLC flash memory devices and the relative performance of various error correction coding techniques. Our initial results indicate that bit errors tend to occur randomly, with no pronounced burstiness or data dependence. We also found that BCH codes achieve a smaller page-error rate (PER) than RS and burst-error correcting codes for a given amount of code redundancy.

This initial investigation represents the cornerstone of a more comprehensive study of error characteristics in flash memory devices and efficient error correction coding strategies to combat them.

References

1. A. Birrell, M. Isard, C. Thacker, and T. Wobber, "A design for high-performance flash disks," *SIGOPS Operating Systems Review*, Vol. 41, No. 2, pp. 88-93, (April 2007).

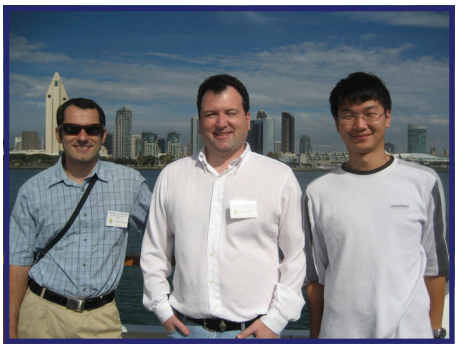
2. Y. Cassuto, M. Schwartz, V. Bohossian, and J. Bruck, "Codes for multi-level flash memories: correcting asymmetric limited-magnitude errors," *Proceedings of IEEE International Symposium on Information Theory*, Nice, France, pp. 1176-1180, (June 2007).

3. E. Gal and S. Toledo, "Algorithms and data structures for flash memories," *ACM Computing Surveys*, Vol. 37, No. 2, pp. 138-163, (June 2005).

4. S. Gregori, A. Cabrini, O. Khouri, and G. Torelli, "On-chip error correcting techniques for new-generation flash memories," *Proceedings of The IEEE*, Vol. 91, No. 4, pp. 602-616, (April 2003).

5. A. Gupta, Y. Kim, and B. Urgaonkar, "DFTL: A Flash translation layer employing demand-based selective caching of page-level address mappings," *Proceedings of the ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2009)*, pp. 229-240, (March 2009).

CMRR Celebrates 25 Years



CMRR students, professors, and attendees of the CMRR Fall Research Review enjoyed a luncheon cruise on San Diego Bay in October 2008 as part of CMRR's 25th celebration.

Selected Papers and Talks

A complete listing of CMRR papers & talks can be found at: http://cmrr.ucsd.edu

Professor Emeritus Ami E. Berkowitz

E. Blackburn, C. Sanchez-Hanke, S. Roy, D.J. Smith, J-I Hong, K.T. Chan, **A.E. Berkowitz**, and S.K. Sinha, "Pinned Co moments in a polycrystalline permalloy/CoO exchange-biased bilayer," *Physical Review B*, Vol. 78, No. 18, (November 2008), pp. 180408 (4).

Professor Emeritus H. Neal Bertram

H.N. Bertram, B. Wilson, and R. Wood, "Error rate expression for perpendicular magnetic recording," *IEEE Transactions on Magnetics*, Vol. 44, No. 10, (October 2008), pp. 2414-2422.

B. Livshitz , **H.N. Bertram**, and **V. Lomakin**, "Precessional magnetization reversal in composite patterned media: Dependence on applied field parameters," *IEEE Transactions on Magnetics,* Vol. 44, No. 11, (November 2008), pp. 3075-3078.

V. Lomakin, S. Li, **B. Livshitz**, A. Inomata, and **H.N. Bertram**, "Patterned media for 10 Tb/in^2 utilizing dual-section "Ledge" elements," *IEEE Transactions on Magnetics,* Vol. 44, No. 11, (November 2008), pp. 3454-3459.

S. Li, **B. Livshitz**, **H.N. Bertram**, A. Inomata, **E.E. Fullerton**, and **V. Lomakin**, "Capped bit patterned media for high density magnetic recording," *Journal of Applied Physics*, Vol. 105, No. 7, (April 2009), pp. 07C122-1-3

B. Livshitz, A. Inomata, **H.N. Bertram**, and **V. Lomakin**, "Analysis of recording in bit patterned media with parameter distributions," *Journal of Applied Physics,* Vol. 105, No. 7, (April 2009), pp. 07C111-1-3.

Professor Eric E. Fullerton

J.W. Seo, **E.E. Fullerton**, F. Nolting, A. Scholl, J. Fompeyrine, and J-P Locquet, "Antiferromagnetic $LaFeO_3$ thin films and their effect on exchange bias," *Journal of Physics: Condensed Matter*, Vol. 20, No. 26, (July 2008), pp. 264014-1-10.

A. Berger, N. Supper, Y. Ikeda, B. Lengsfield, A. Moser, and **E.E. Fullerton**, "Improved media performance in optimally coupled exchange spring layer media," *Applied Physics Letters,* Vol. 93, No. 12, (September 2008), pp. 122502-1-3.

J. McCord, Y. Henry, T. Hauet, F. Montaigne, **E.E. Fullerton**, and S. Mangin, "Mechanism of chirality reversal for planar interface domain walls in exchange-coupled hard/soft magnetic bilayers," *Physical Review B*, Vol. 78, No. 9, (September 2008), pp. 094417-1-5.

C. Burrowes, D. Ravelosona, C. Chappert, S. Mangin, **E.E. Fullerton**, J.A. Katine, and B.D. Terris, "Role of pinning in current driven domain wall motion in wires with perpendicular anisotropy," *Applied Physics Letters*, Vol. 93, No. 17, (October 2008), pp. 172513-1-3.

A.K. Chesnel, **E.E. Fullerton**, M.J. Carey, J.B. Kortright, and S.D. Kevan, "Magnetic memory in ferromagnetic thin films via exchange coupling," *Physical Review B* , Vol. 78, No. 13, (October 2008), pp. 132409-1-4.

Professor Paul H. Siegel

D. Bickson, D. Dolev, O. Shental, **P.H. Siegel**, and **J.K. Wolf,** "Gaussian belief propagation based multiuser detection," *ISIT 2008*, Toronto, Canada, (July 2008), pp. 1878-1882.

O. Shental, **P.H. Siegel**, **J.K. Wolf**, D. Bickson, and D. Dolev, "Gaussian belief propagation solver for systems of linear equations," *ISIT 2008*, Toronto, Canada, (July 2008), pp. 1863-1867.

E. Yaakobi, A. Vardy, **P.H. Siegel**, and **J.K. Wolf**, "Multidimensional flash codes," *46th Annual Allerton Conference*, (September 2008), pp. 392-399.

M-H.N. Taghavi and **P.H. Siegel**, "Adaptive methods for linear programming decoding," *IEEE Transactions on Information Theory*, Vol. 54, No. 12, (December 2008), pp. 5396-410.

Professor Frank E. Talke

M. Chung, Y-C. Wu, and **F.E. Talke**, "Film thickness dependence of lubricant mobility," *Tribology Letters,* Vol. 32, No. 1, (October 2008), pp. 35-41.

B. Raeymaekers and **F.E. Talke**, "Measurement and sources of lateral tape motion: A review," *ASME Journal of Tribology*, Vol. 131, No. 1, (January 2009), pp. 011903-1-6.

M. Duwensee, S. Suzuki, J. Lin, D. Wachenschwanz, and **F.E. Talke**, "Direct simulation Monte Carlo method for the simulation of rarefied gas in discrete track recording Head/Disk Interfaces," *ASME Journal of Tribology,* Vol. 131, No. 1, (January 2009), pp. 012001-1-7.

H. Li, H. Zheng, Y. Yoon, and **F.E. Talke**, "Air bearing simulation for bit patterned media," *Tribology Letters,* Vol. 33, No. 3, (March 2009), pp. 199-204.

(Continued from page 12)

H. Li, C-T Yin, and **F.E. Talke**, "Thermal insulator design for optimizing the efficiency of thermal flying height control sliders," *Journal of Applied Physics,* Vol. 105, No. 7, (April 2009), pp. 07C122-1-3.

B. Raeymaekers and **F. E. Talke**, "Attenuation of lateral tape motion due to frictional interaction with a cylindrical guide," *Tribology International*, Vol. 42, No. 5, (May 2009), pp. 609-614.

Professor Jack K. Wolf

Z. Wu, **P.H. Siegel, J.K. Wolf,** and **H.N. Bertram**, "Mean-adjusted pattern-dependent noise prediction for perpendicular recording channels with nonlinear transition shift," *IEEE Transactions on Magnetics*, Vol. 44, No. 11, (November 2008), pp. 3761-3764.

R. Gabrys and **J.K. Wolf**, "Modifications to the Lagrange interpolation method of decoding Reed Solomon codes," *2008 International Symposium on Communications and Information Technologies (ISCIT). IEEE,* Lao China, (October 2008), pp. 459-63.

J.K. Wolf, "Signal processing for digital recording on patterned media," *2nd International Conference on Signals, Circuits and Systems,* Monastir, Tunisia, (November 2008), pp. 1-6.

I. Demirkan, **P.H. Siegel**, and **J.K. Wolf**, "Error event characterization on 2-D ISI channels," *IEEE Transactions on Information Theory*, Vol. 55, No. 3, (March 2009), pp. 1146-1152.

Graduate Students & Researchers Near Completion

Student	Level	Advisor	Dept	Research	Completion
Ralf Brunner	Ph.D.	Talke	MAE	Carbon coating and lubrication studies for wear protection of the head/disk interface	Spring 2009

The Spring 2009 Research Review and Advisory Council Meeting will be held on May 11-12, 2009. For further information on the CMRR Research Review, please contact Betty Manoulian at 858-534-6707 or bmanoulian@ucsd.edu .

CMRR Research Review Highlights

The Fall Research Review held in October 2008 was a well attended success. Over 35 people from CMRR Industrial Sponsor companies and other invited guests participated in the meeting, including several who participated via teleconference.

In addition to the sessions devoted to technical presentations of CMRR research results, the Review featured a special presentation by Dr. Charles Rettner entitled "Application of Electron Beam Lithography to the Development and Fabrication of Prototype 'Storage Class' Memory Devices."

CMRR Sponsor company employees may access the abstracts and viewgraphs of all Research Review presentations on the CMRR website in the Sponsor Resources section at http://cmrr.ucsd.edu/sponsors/ Contact Jan Neumann with any questions regarding Sponsor Resources at jneumann@ucsd.edu .

Graduate Degree Awarded

Zheng Wu, a CMRR student co-advised by Professors Paul Siegel and Jack Wolf, received her Ph.D. in December 2008. Her dissertation was entitled "Channel Modeling, Signal Processing and Coding for Perpendicular Magnetic Recording." Zheng is currently a Staff Engineer, at Link-A-Media Devices in Santa Clara, California.

New Postdoctoral Scholars

Dr. Melanie Gauvin is a new postdoctoral scholar in Professor Frank Talke's lab. She received her masters degree in physics from the Ecole Normale Superieure de Lyon in 2005. In 2008, she was awarded a Ph.D. in material science from the Ecole Centrale de Lyon. Her thesis, entitled "In Situ Analytical Approach of Zinc Phosphate Anti-Wear Mechanism," contributed to a fundamental understanding of pressure-induced effects on anti-wear additive atomic structure in boundary lubricated contacts. At CMRR, Melanie will investigate carbonless overcoats. Outside of work Melanie enjoys jogging, scuba-diving and outdoors sports in general.

Dr. Ido Tal has joined Professor Paul Siegel's group as a postdoctoral scholar. He received his B.Sc., M.Sc., and Ph.D. degrees in computer science from Technion---Israel Institute of Technology, Haifa, Israel, in 1998, 2003 and 2009, respectively. His research interests include constrained coding and error-control coding.

New Graduate Student

Lynn E. Greiner is a first year graduate student who recently joined Professor Paul Siegel's group. He is currently working in conjunction with both Professor Siegel and Dr. Frederick Spada on "Data Reconstruction from Degraded Recording Media." From 2006-08, he worked under Dr. Spada on the "Secure Erase" project. He received his B.S. degree in electrical engineering and is currently pursuing his M.S. at the University of California, San Diego.

Gifts, Grants and Awards

Professors **Paul H. Siegel** and **Alexander Vardy** received funding from the UC Lab Fees Research Program for their project entitled "Coding, Detection, and Inference in Multiple Dimensions."

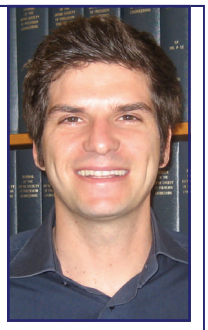
Under the Secure Erase Project, **Fred Spada**, **Paul H. Siegel** and **Steven Swanson** received support from NSA for their work on data reconstruction, flash memory secure erase, and thermal stability.

INSIC/Tape Program awarded **Paul H. Siegel's** proposal "Modified Code Concatenation Architectures using Generalized Error Locating Codes," and **Fred Spada's** proposal "Comparison of Tapes and Deposition/Erosion Mitigation Studies."

Uwe Boettcher, a CMRR graduate student, received travel support from INSIC to attend EHDR meetings.

Visitors

Peter Kroetz is a visiting student from Germany in Professor Frank Talke's lab. He is currently completing his Bachelor's thesis from the Ilmenau Technical University in Germany. His fields of interest are carbon coatings and their creation, characterization, and tribological properties. In his free time, Peter enjoys sports, such as, swimming, jogging, and soccer, as well as relaxing at the beach and spending time with his friends.



Marco Papaleo is a visiting graduate student under Professor Paul Siegel and Professor Jack Wolf. He received his B.S. and M.Sc. degrees (summa cum laude) in telecommunication engineering from the University of Bologna, Italy, in 2003 and in 2006, respectively. He received an award for one of the three best theses in telecommmunication engineering from University of Bologna for the academic year 2004-05. In January 2006, he joined the Advanced Research Center on Electronic Systems for Information and Communications Technologies "Ercole De Castro" (ARCES) at the University of Bologna, where he also began his Ph.D. studies in 2007. In the summer of 2008 he was a visiting Ph.D. student at the German Aerospace Center (DLR) Institute of Communications and Navigation in Wessling. He was involved in the design and analysis of LDPC convolutional codes. In 2006, he was a visiting affiliate student at the University College of London (UCL), in England. His current research activities are focused on the next generation wireless telecommunication systems, for both terrestrial and satellite networks. In particular, he is interested in the design and performance evaluation of error control coding (with emphasis on packet level coding).

Student Awards

Ali Karimian, a Teaching Assistant for CMRR Professor Eric Fullerton received an Outstanding Tutor Award for the Fall Quarter 2008.

Tasha Vanesian, a graduate student in the ECE Department has received the Teaching Assistant Excellence Award for the Fall Quarter 2008. Tasha works with CMRR Project Scientist Gordon Hughes.

Each quarter, the ECE Department recognizes students who excel in their teaching services and provide a valuable contribution to teaching at UCSD.

CMRR
Center for Magnetic Recording Research

CMRR Director:
Paul H. Siegel

Newsletter Editor:
Jan Neumann James

Photography:
Ray Descoteaux
Betty Manoulian

Contributors:
Nate Heintzman
Jan Neumann James
Betty Manoulian
Paul Siegel
Iris Villanueva

http://cmrr.ucsd.edu

The Incredible Shrinking Hard Drive

On April 4th 2009, UCSD's Center for Magnetic Recording Research was among hundreds of exhibitors at the first ever San Diego Science Festival, held at Balboa Park. An audience well in excess of fifty thousand people packed the park to learn about the incredible science and engineering innovations occurring in San Diego, including the ground-breaking research conducted by CMRR and the Center's industry partners.

Left to Right: Graduate students Seyhan Karakulak & Uwe Boettcher and CMRR Visitors Sebastian Helm & Peter Kroetz

In an exhibit called "The Incredible Shrinking Hard Drive," CMRR students and staff wowed people of all ages with video displays, model hard drives of increasing storage capacity and decreasing size, and live demonstrations of open hard drives in action. Exhibit participants from CMRR were Uwe Boettcher, Ralf Brunner, Nate Heintzman, Sebastian Helm, Seyhan Karakulak, Betty Manoulian, Eitan Yaakobi, Aravind Iyenger, and Peter Kroetz. For more information about the Science Festival please visit http://www.sdsciencefestival.org/, and for more information about CMRR's exhibit, please email Nate Heintzman at nheintzm@ucsd.edu

CMRR
University of California, San Diego
Center for Magnetic Recording Research, 0401
9500 Gilman Drive
La Jolla, CA 92093-0401